A Precise Clock Distribution Network

for MRPC-based Experiments

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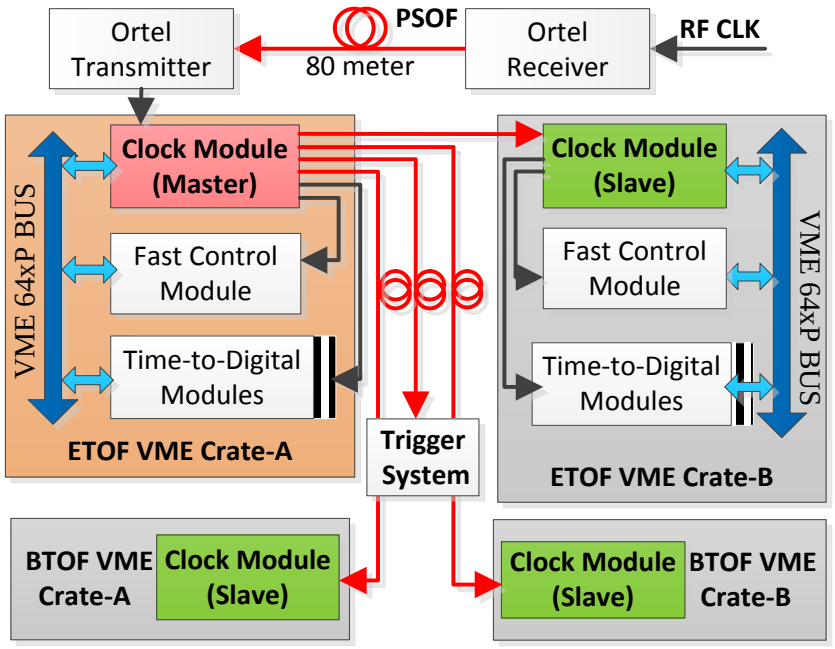
Outline

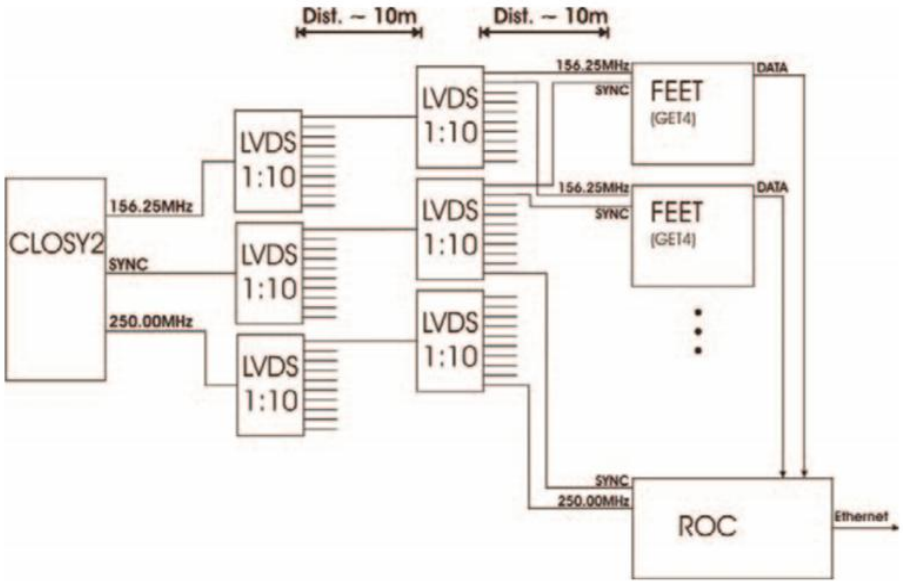
- 1. Introduction
- 2. Proposed Clock System
  - System design
  - Module design
  - Phase measurement
- 3. Test Result
- 4. Conclusion & Next Plan

1. Introduction

- MRPC
  ——Multi-Gap Resistive Plate Chamber
- Application
  - BESIII (Beijing Spectrometer III) TOF (Time of Flight)
  - STAR (STAR Detector) TOF
  - CBM (Compressed Baryonic Matter) TOF
- Future
  ——With much more channels and larger scale

Clock distribution in BESIII TOF



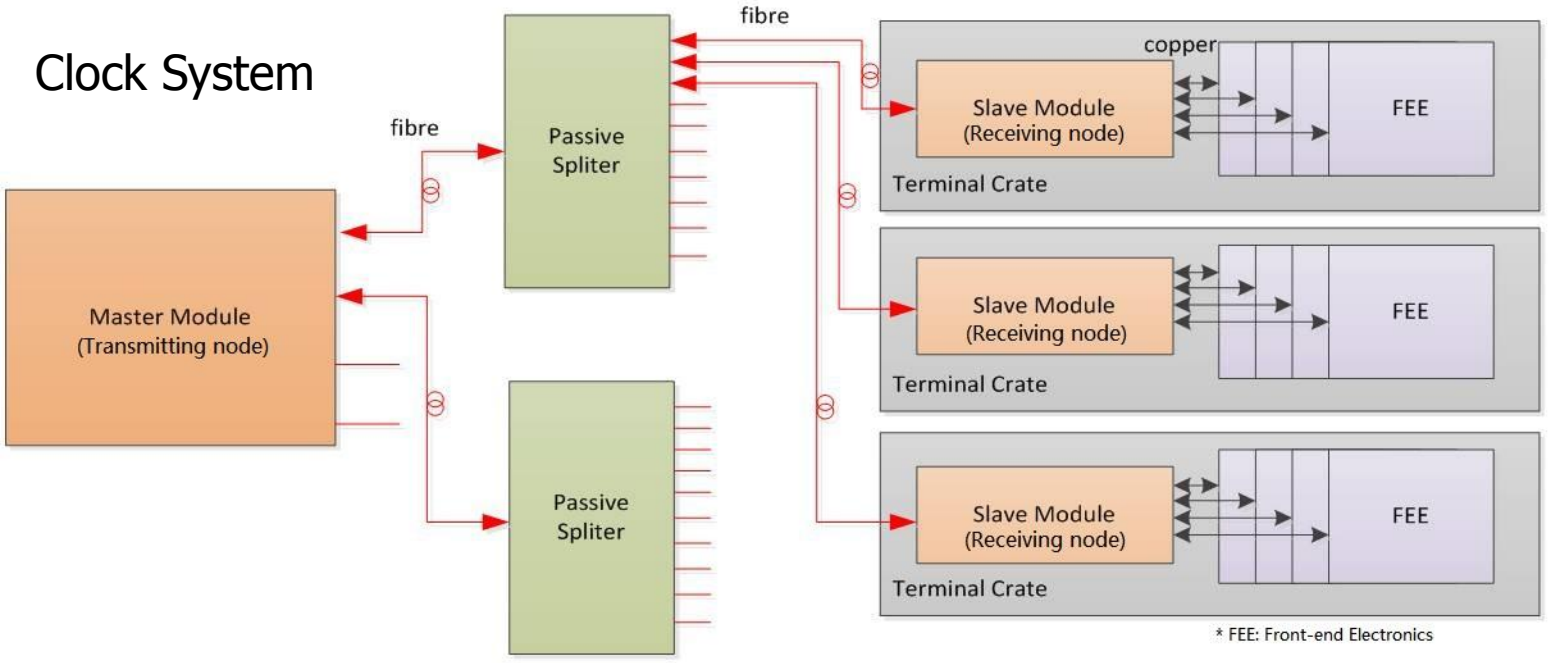


Clock distribution in CBM TOF wall

In this design

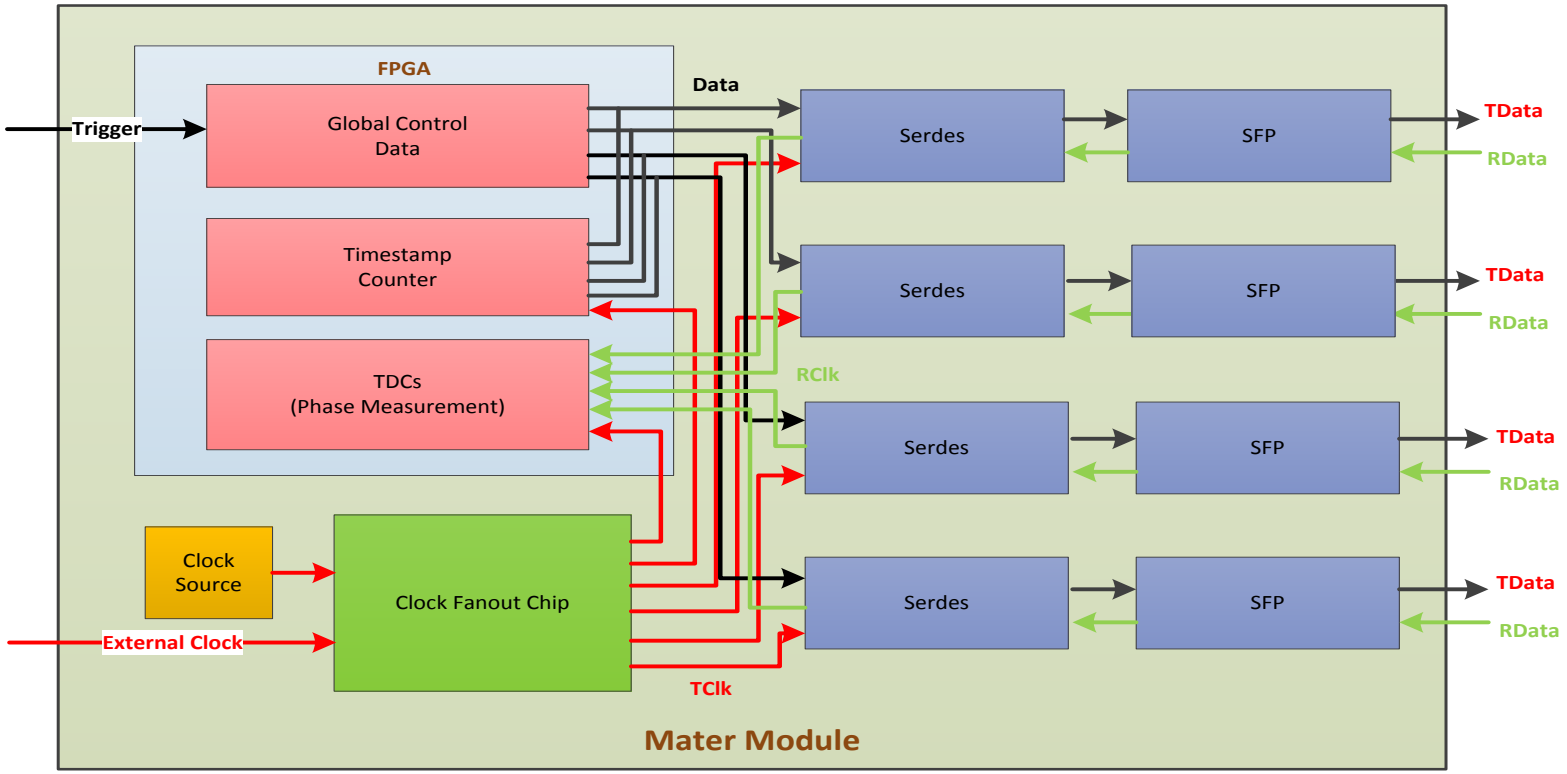
- Tree-cascade structure
- Global command coded with clock signal

2. Proposed Clock System



- Tree-cascade structure
- Bidirectional serial interconnection
- TDM (time division multiplexing)
  - Send request command
  - Distribute Time window

Mater Module Design



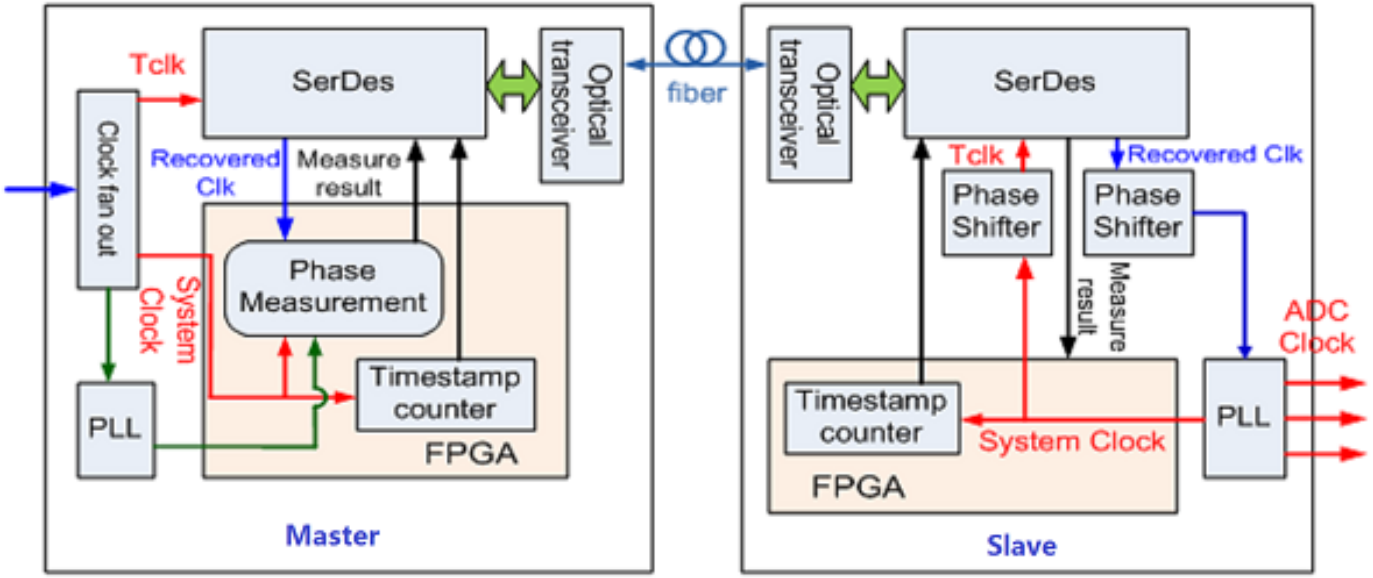
- The master clock module mainly consists of optical transmission, FPGA and clock generation circuits.
- The slave module has function of clock recovery, jitter reduction and clock fan-out circuit. It provides system clock to other electronics in the same crate.

Clock Synchronization

- Frequency
- Delay

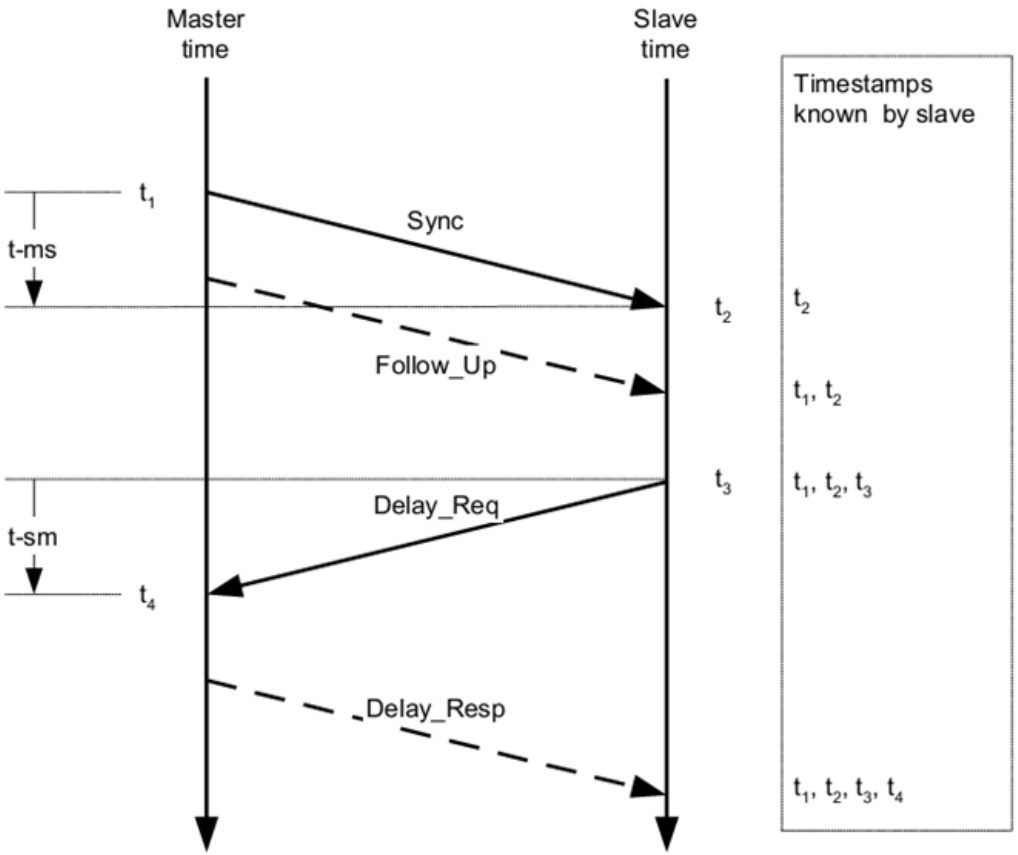
$$Delay_{TR} = Coarse_{TR} + Phase_{TR}$$

- $Coarse_{TR}$ (r-PTP)
- $Phase_{TR}$ (DDMTD)



** P. Moreira and J. Serrano et al., "White rabbit: Sub-nanosecond timing distribution over ethernet," in Proc. IEEE Int. Symp. Precision Clock Synchronization for Measurement Control and communication, Brescia, Italy, Oct. 2009, pp. 1–5.*

r-PTP (reduced version of Precision Time Protocol)



$T2 = T1 + T_{delay} + T_{offset}$

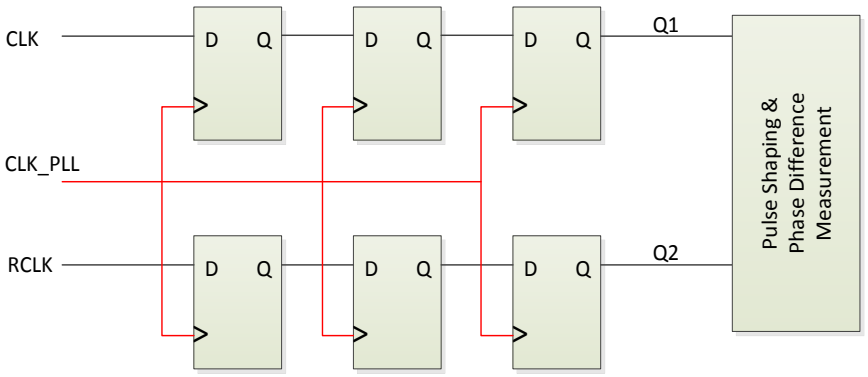
$T3 = T4 - T_{delay} + T_{offset}$

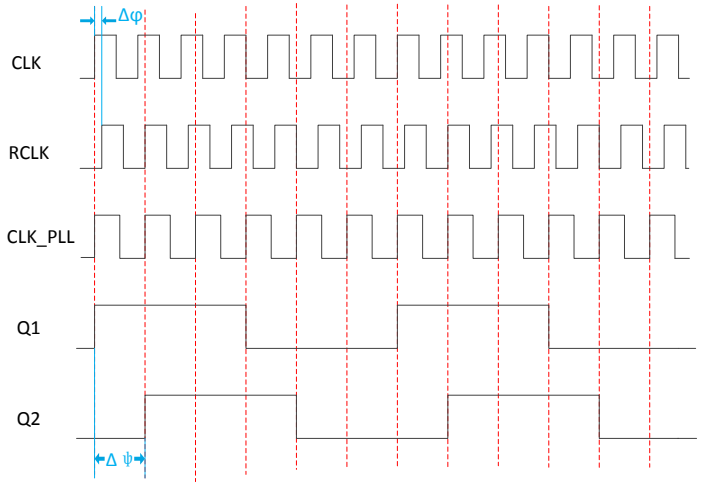
$T_{offset} = (T2-T1+T3-T4) / 2$

$T_{delay} = (T2-T1-T3+T4) / 2$

DDMTD (Digital Dual Mixer Time Difference)

$$f_{clk\_pll} = \frac{n}{n+1} f_{clk}$$



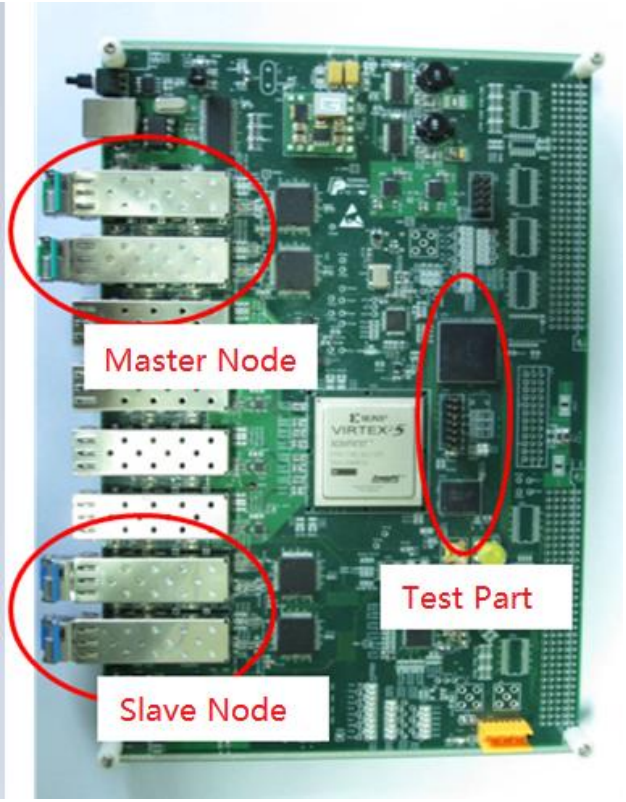


$$\Delta\psi = n\Delta\varphi$$

After repeated experiments in laboratory, the measurement error of the phase difference is less than 100ps when the sample number is determined to be 10^5.

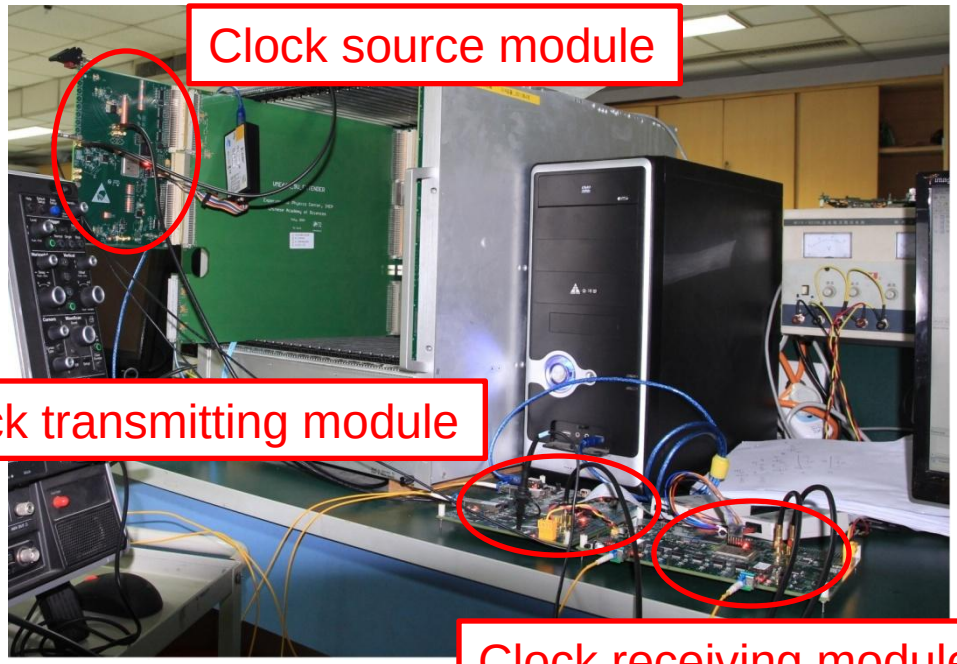
Photos of testing modules

Clock Source Module



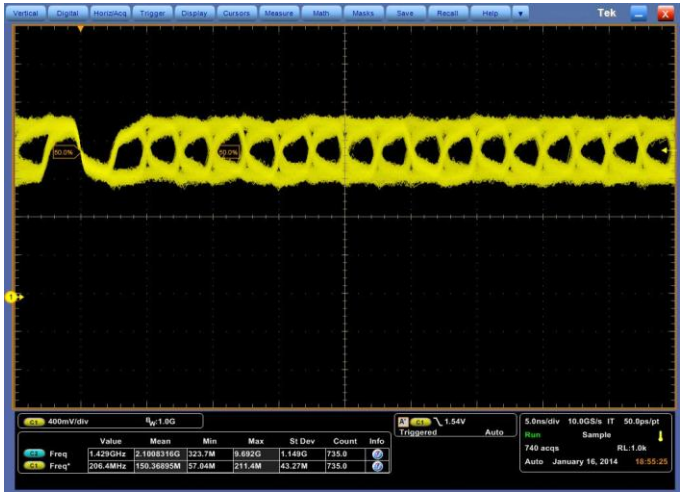
Clock Transmitting & Receiving Module

3. Test Result

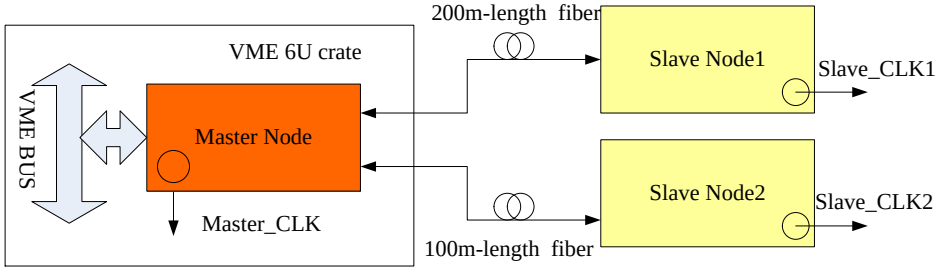


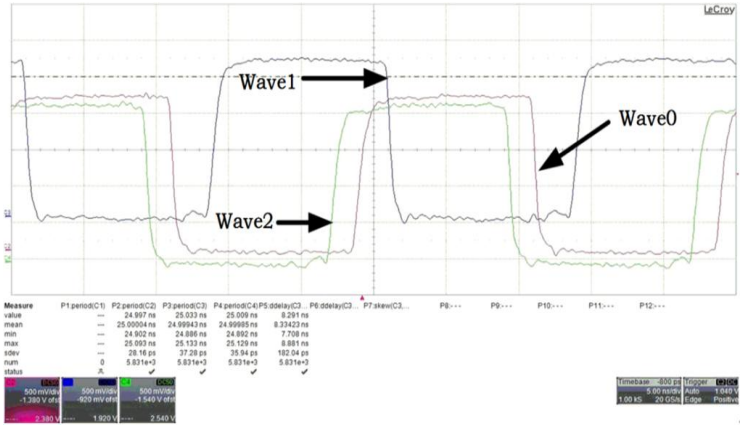
System Clock Jitter:
less than 20ps.

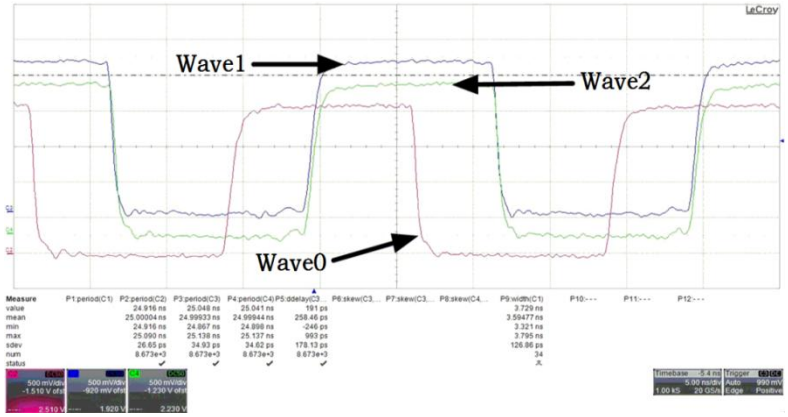
Transmit and receive data effectively.



Clock synchronization test

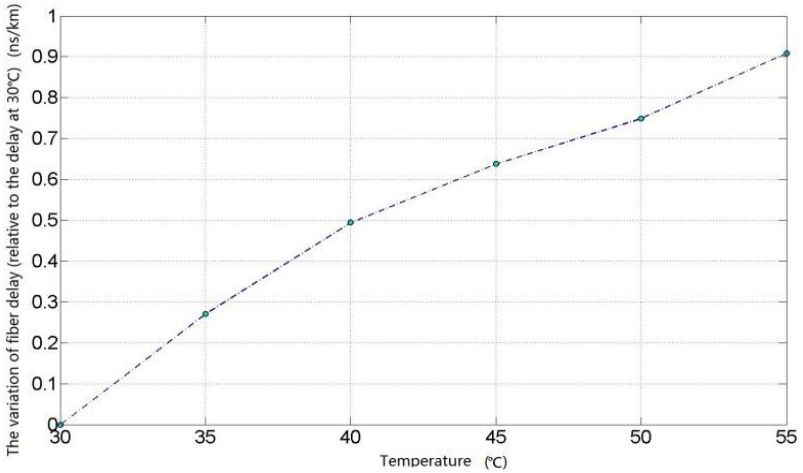




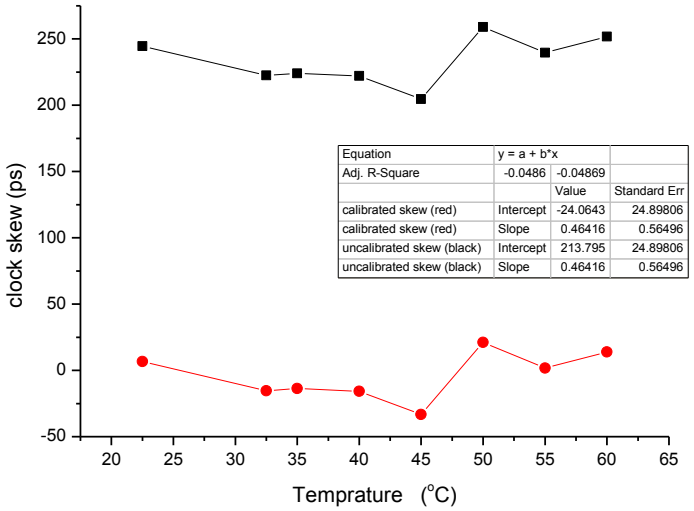


The waveform of slave clock before (left) and after (right) phase adjustment.
Wave 0：master clock, Wave 1：slave clock1, Wave2：slave clock2.

The variation of fiber delay



The variation of clock skews



- Temperature: 22.5℃~60 ℃.
- The delay caused by temperature drift should be 270ps when the temperature changes 37.5 ℃ theoretically.
- After the calibration of the transfer delay, the clock skew between two channels on receiving module varies in the range -21.08~33.24ps.

4. Conclusion & Next Plan

- Advantages:
  - High performance of distributed clock (Jitter<20ps, Skew<100ps)
  - Efficient transmission link for both data and clock
  - Flexible capability for system expansion

- Next Plan:
  - TDM (time division multiplexing) implementation
  - A complete system for real-time monitoring

Thank you!