The Semi-Digital Hadronic CALorimeter (SDHCAL) for futur leptonic colliders

RPC 2016 - 23 February 2016

Antoine Pingault - UGent
On Behalf of the CALICE-SDHCAL Group
IPNL, LPC, GWNU, UGent, CIEMAT, UCL & NCEPU

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The Cube

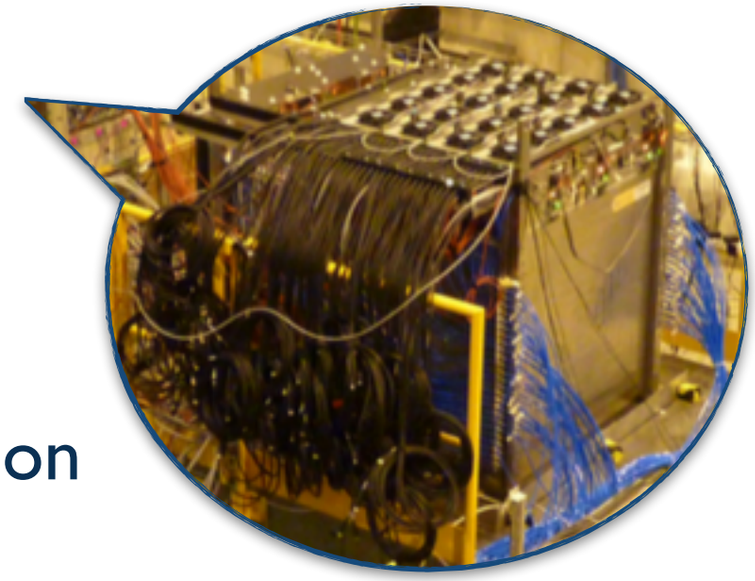
Semi Digital Hadronic CALorimeter

Semi Digital = 3 Thresholds detection

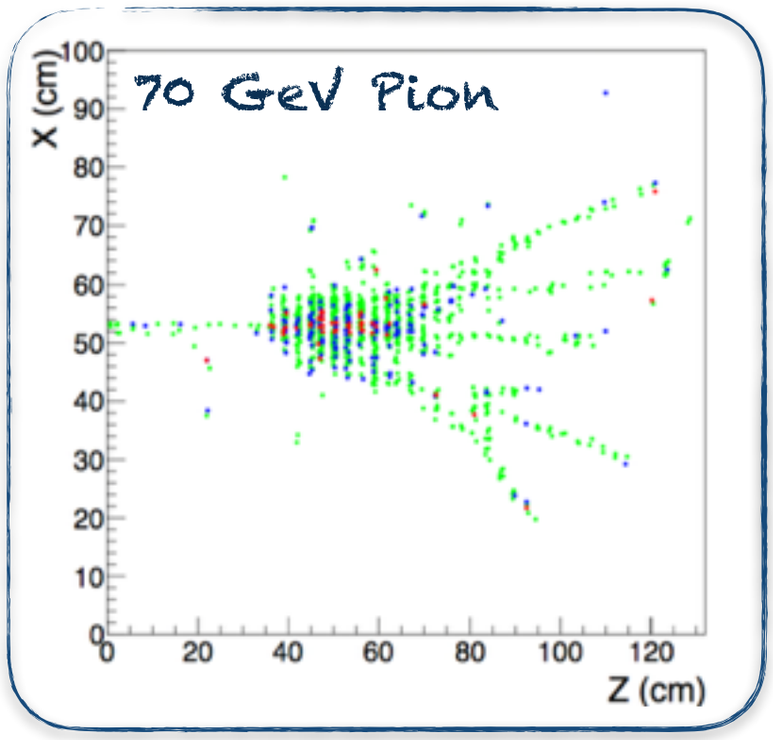
48 Layers of **1x1m²** gRPC + Steel Structure

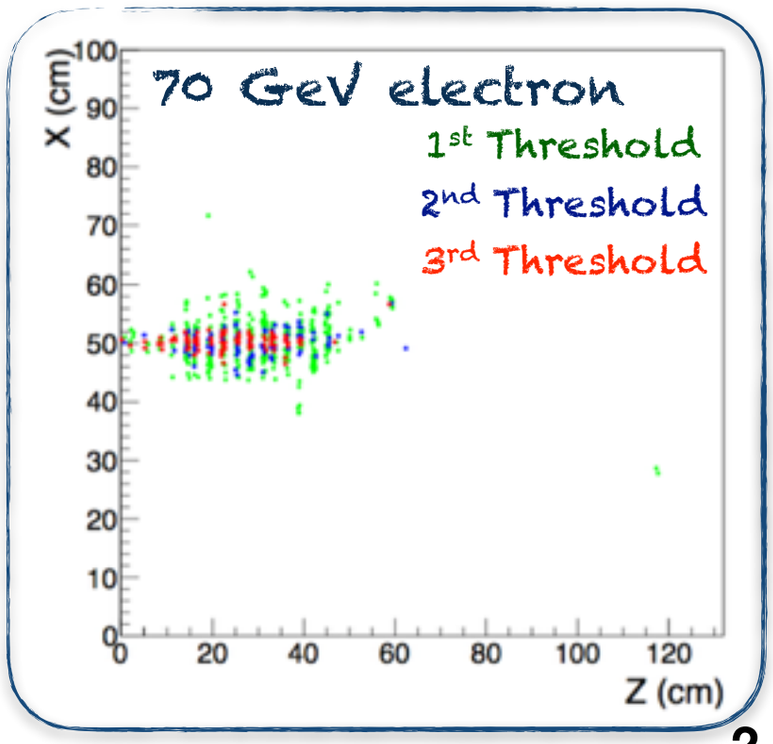
~0.5M channels, power pulsed & trigger less acquisition

Dead zone < 2%



Event View





CALICE Calorimeter for ILC

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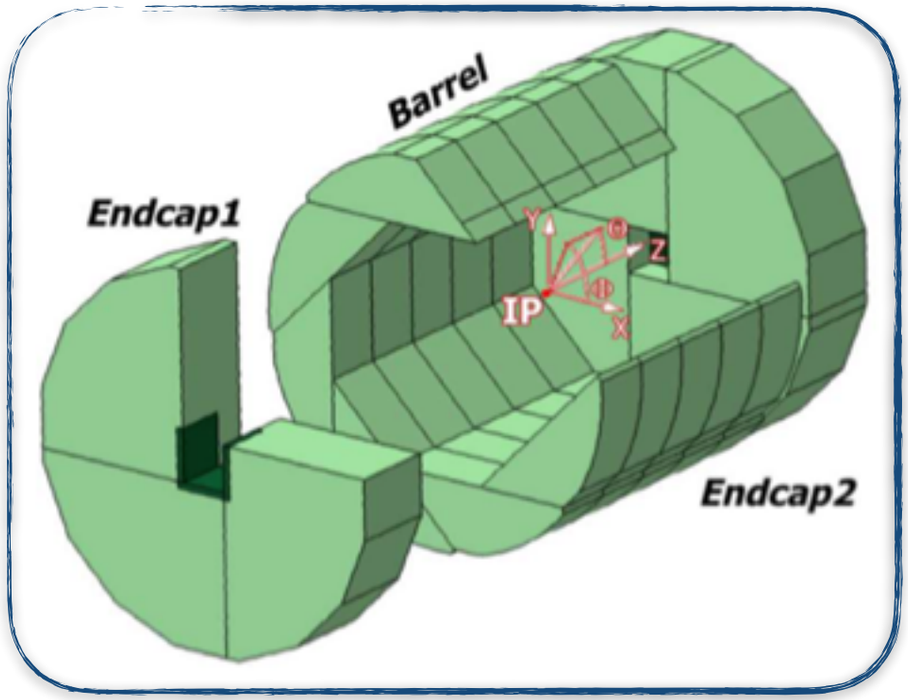
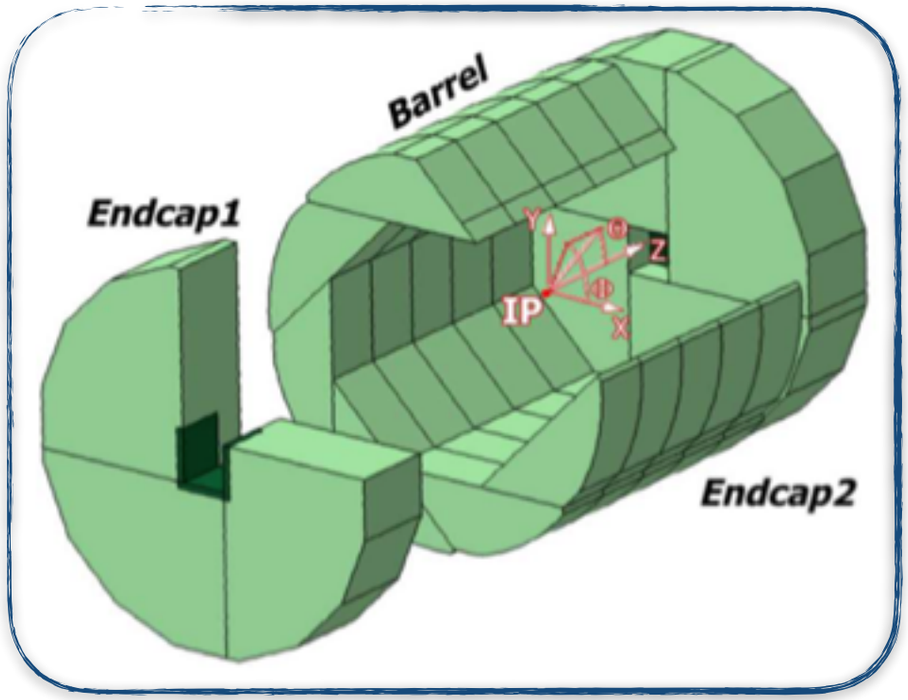
SDHCAL - What's next

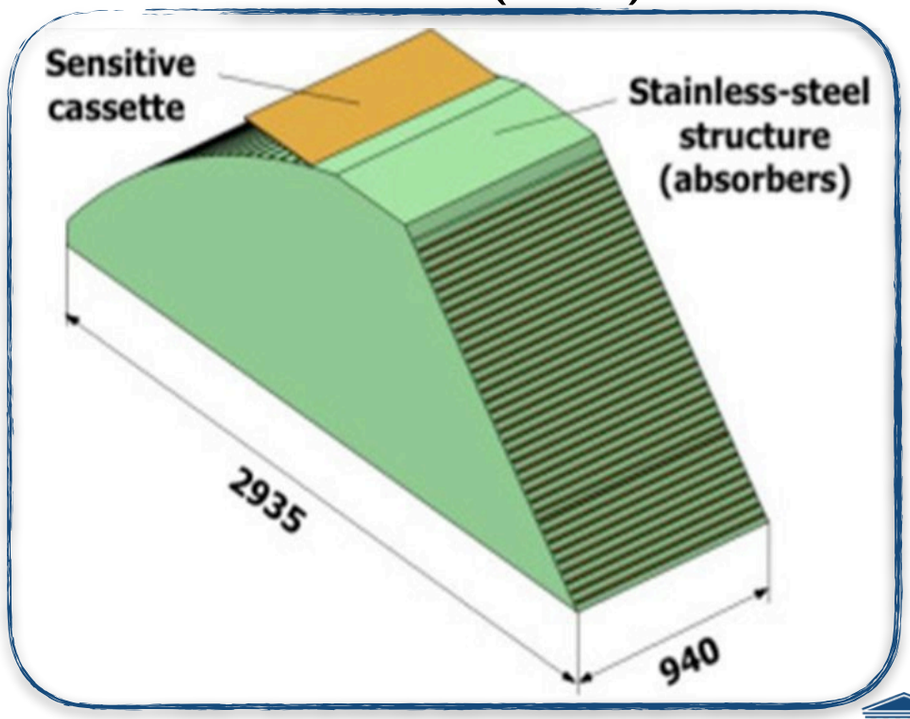


Videau geometry (up)

SDHCAL - What's next



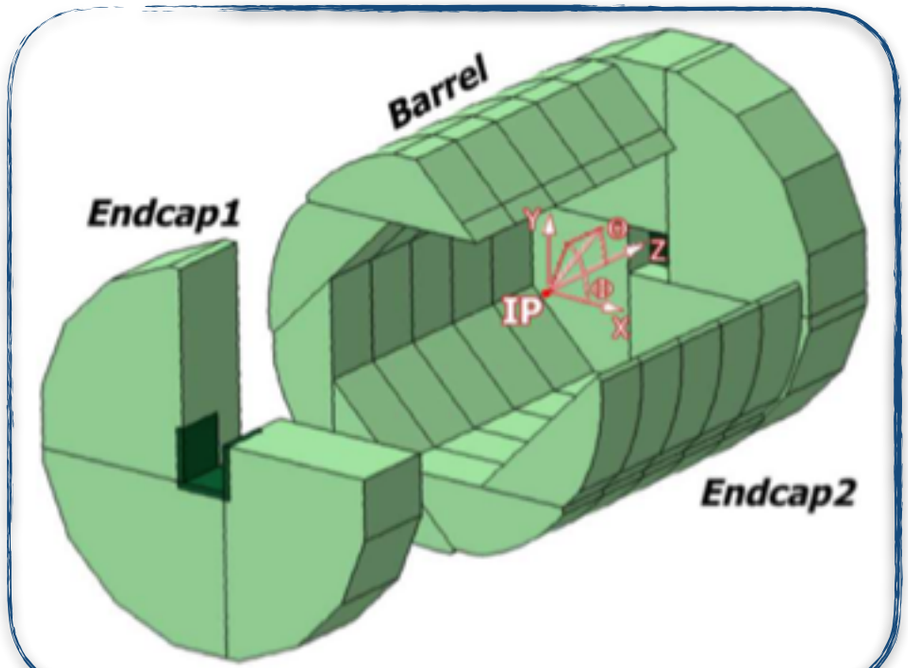
Videau geometry (up)
& module (down)



SDHCAL - What's next

EndGoal: Feasibility of "Videau" module

↳ Chambers up to ~**3x1m²**



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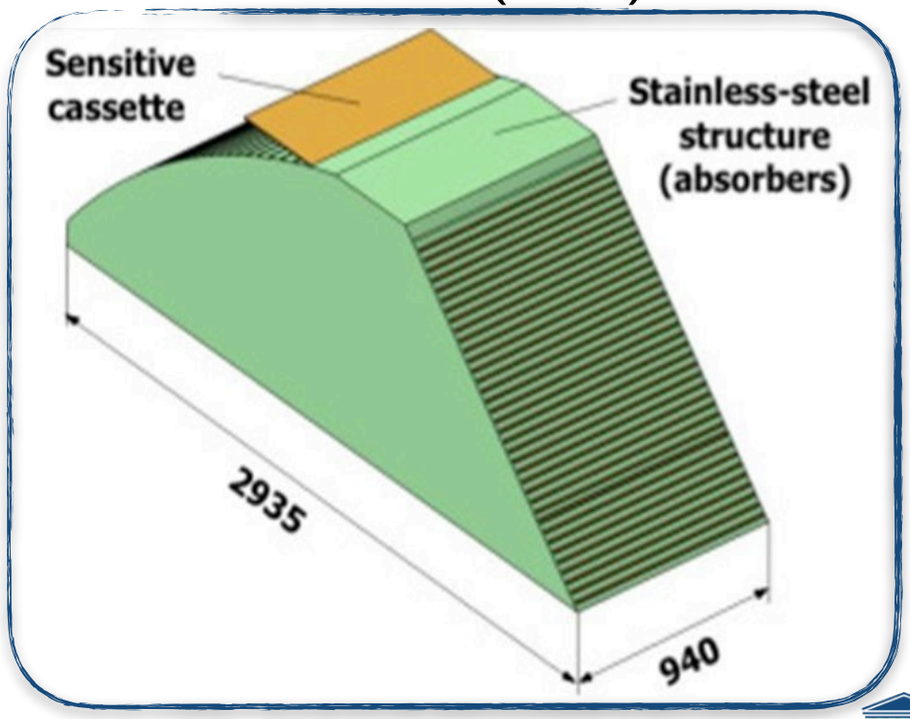


SDHCAL - What's next

EndGoal: Feasibility of "Videau" module

↳ Chambers up to ~**3x1m²**

2016 - 2017 Goal :

2x1m2 chambers (4-5)

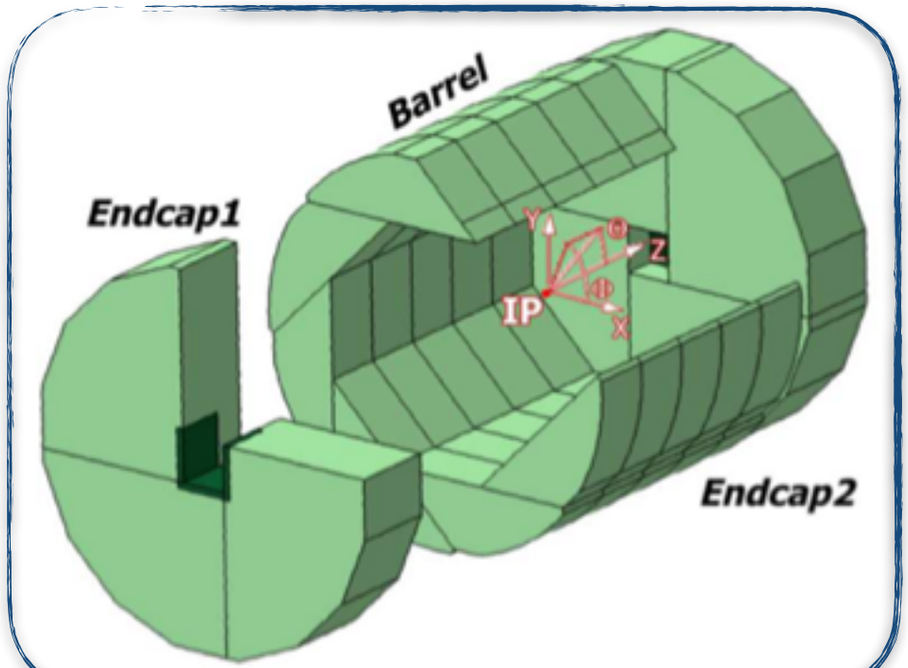
New gas distribution system

New electronics

New Mechanical Structure

Combined TB with ECAL

Gas recycling system



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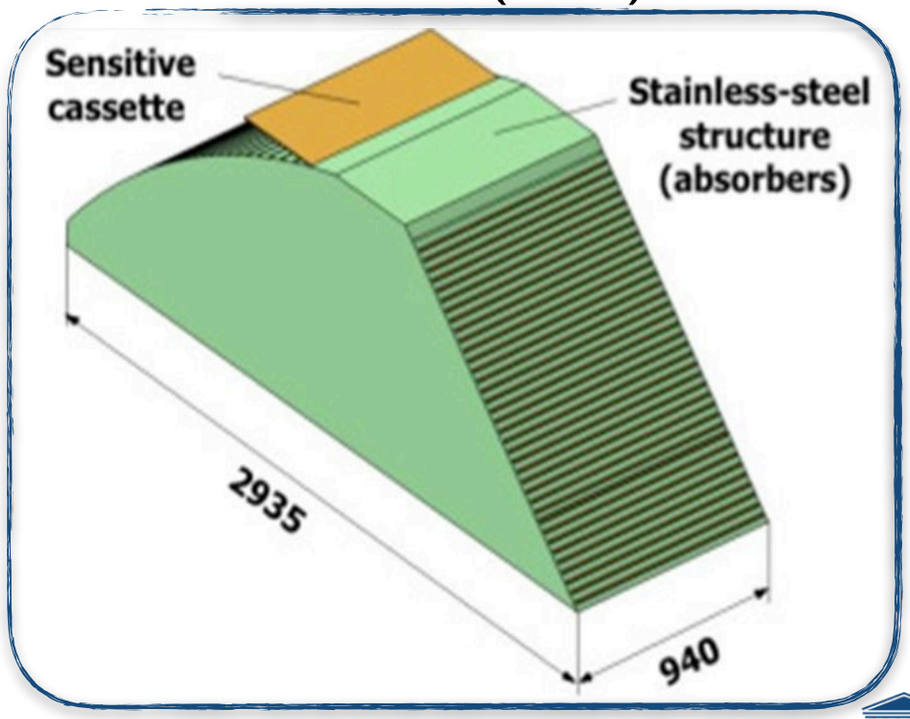

Make it bigger

Double chamber size : 2x1m^2

Unchanged overall construction process…

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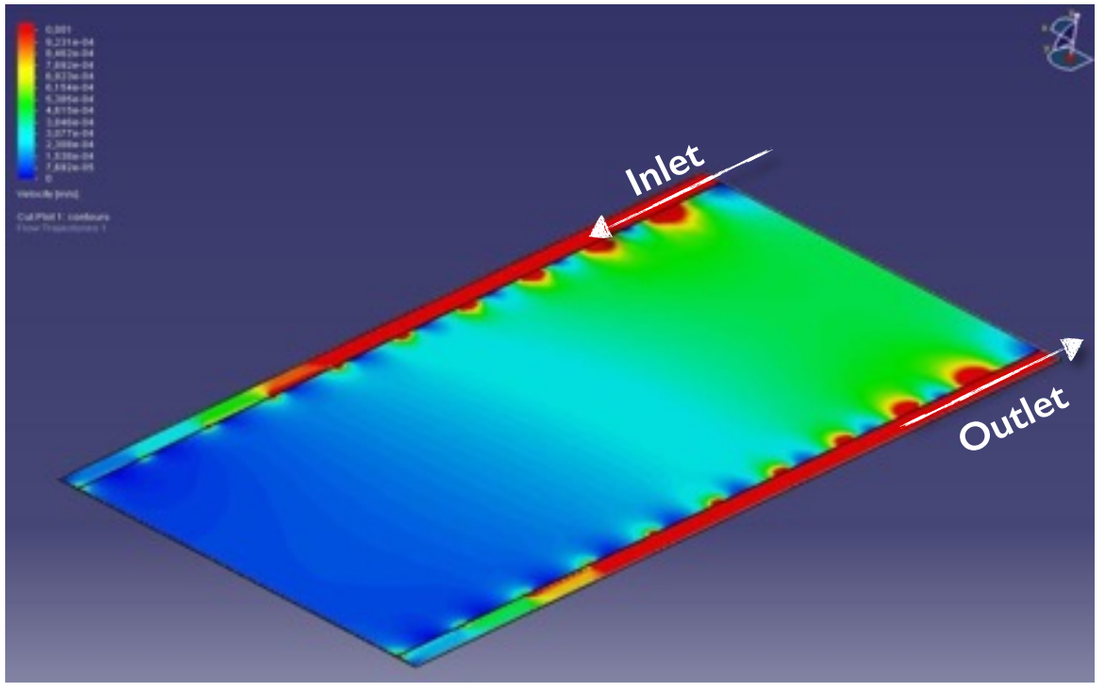
… But for gaz the circulation

↳ Need homogeneity : Efficiency - Multiplicity



Gaz circulation simulation in 2x1m2 chambers,
Old (left) & new (right) schemes

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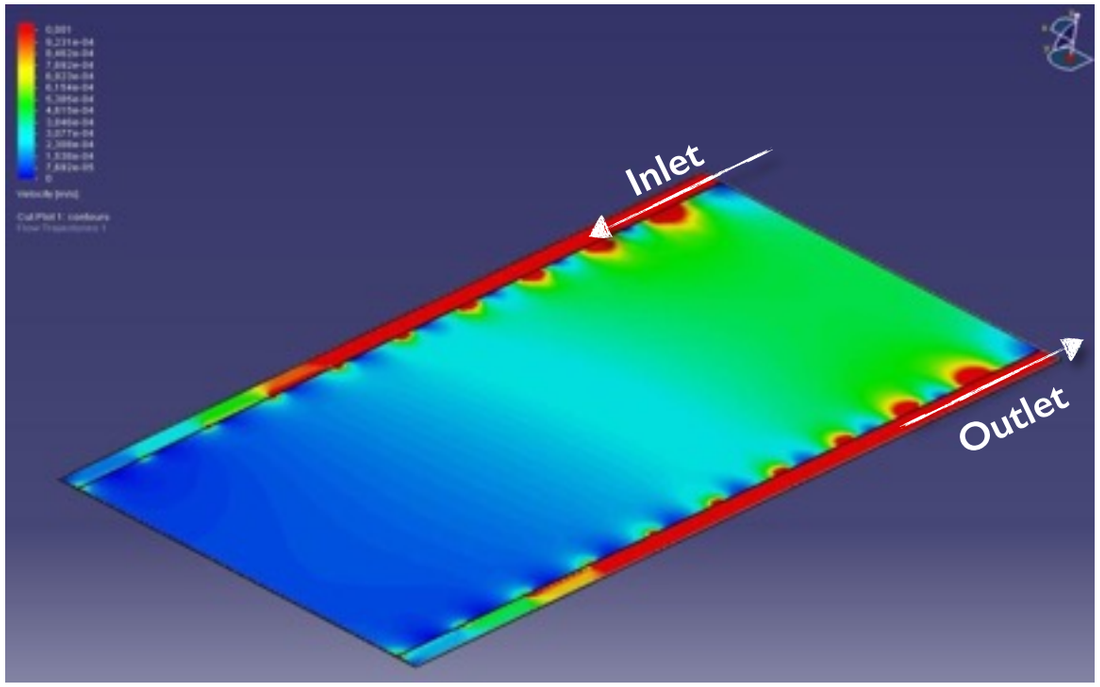
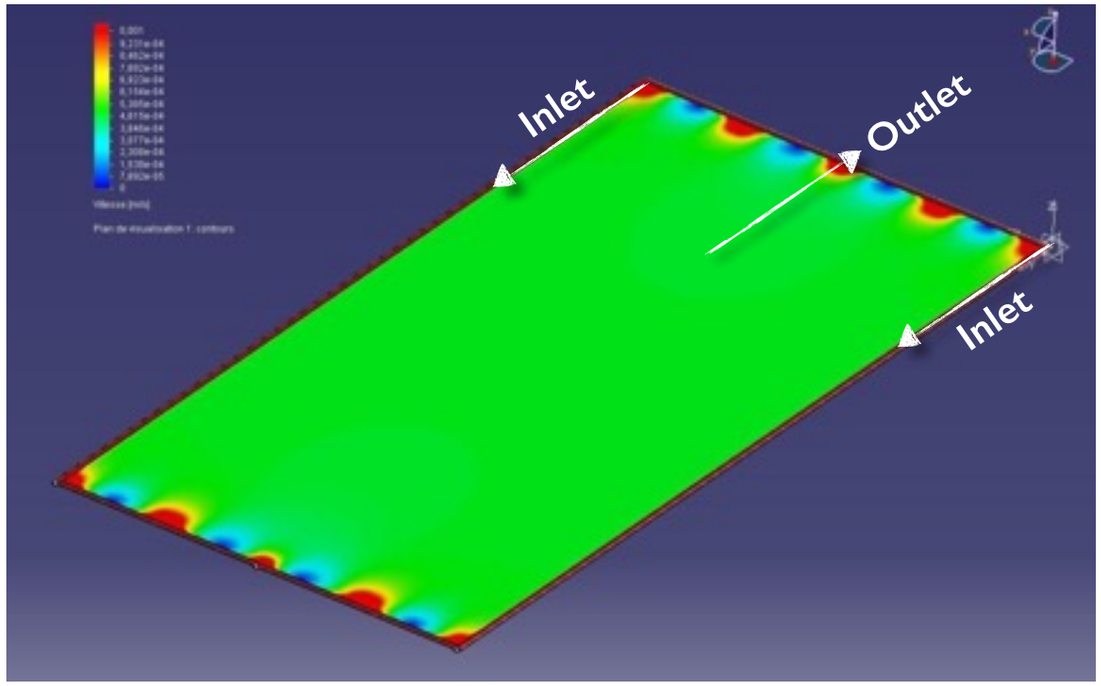




Gaz circulation simulation in 2x1m2 chambers,
Old (left) & new (right) schemes

The (current) Electronics

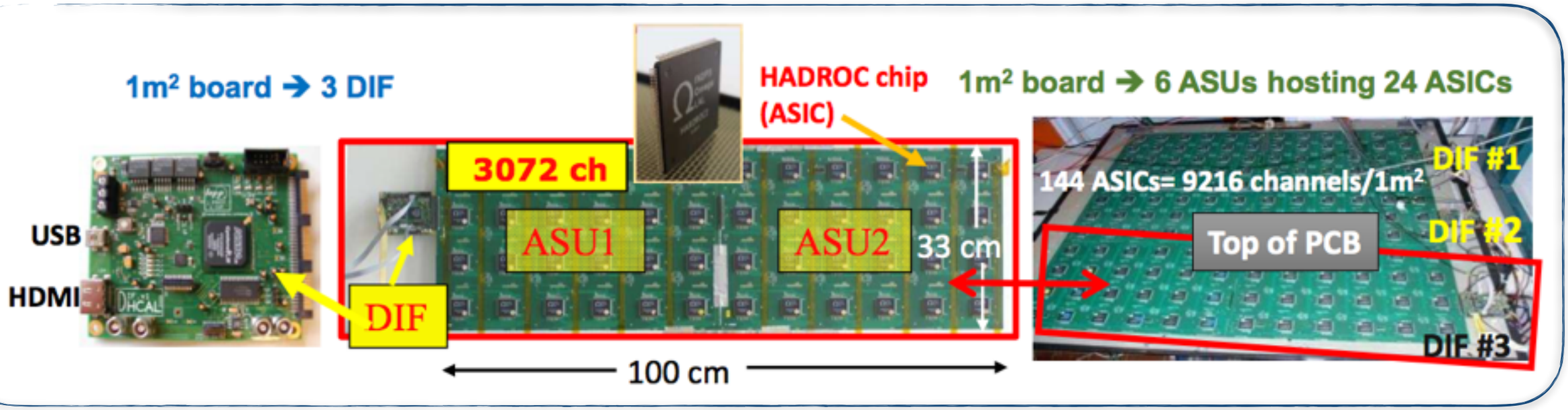
One chamber:

3 DIFs (1 per Slab of 2 ASU)

6 ASUs 50x33cm

144 ASICs (Hardroc2)

9216 Channels (1x1cm2 copper pads)



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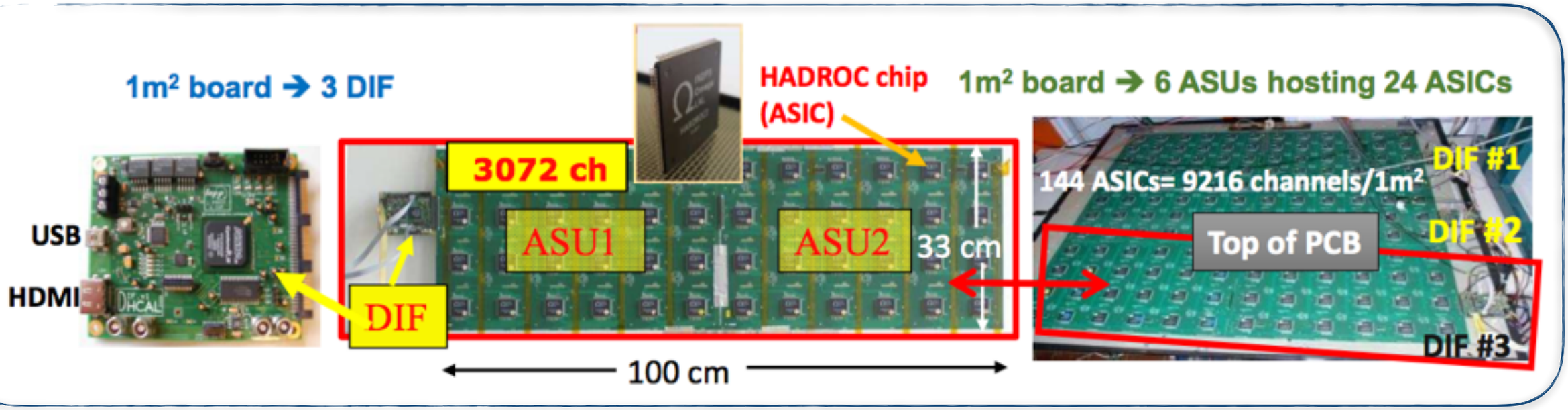
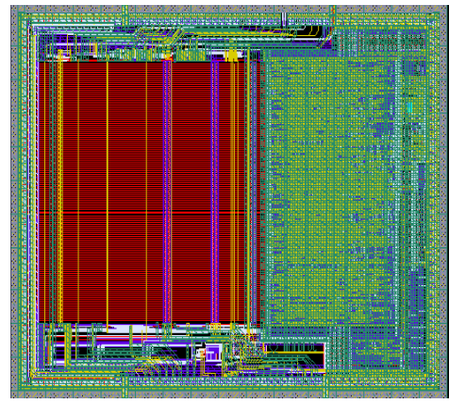


Everything is embedded in the cassette!

New Electronics - ASIC

New ASIC : **HARDROC3** (AMS SiGe 0.35µm)



HR3 schematics

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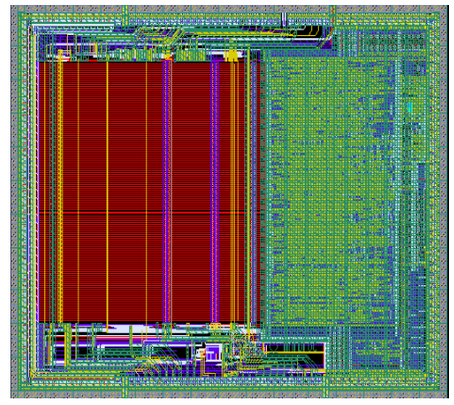

HR3 schematics

Updated to comply with ILD demands:

- 64 independant channels (zero suppression)
- Extended dynamic range (up to 50pC)
- I2C protocol for slow control parameters
- Internal fast clock generator
- Fallback: HARDROC2 emulation

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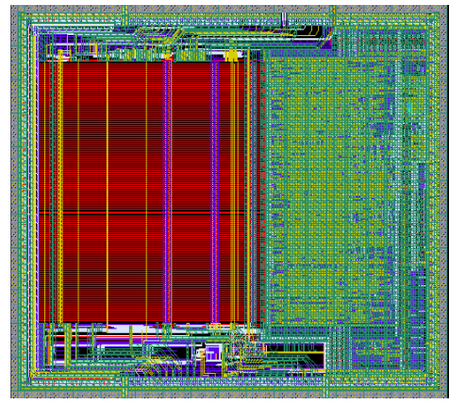

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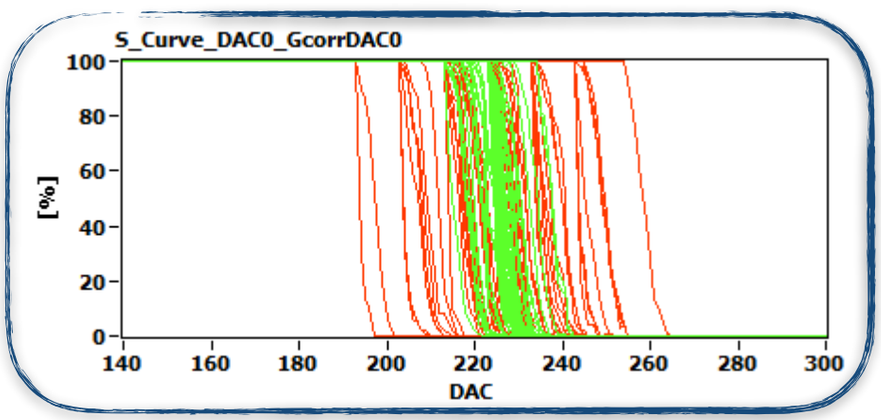
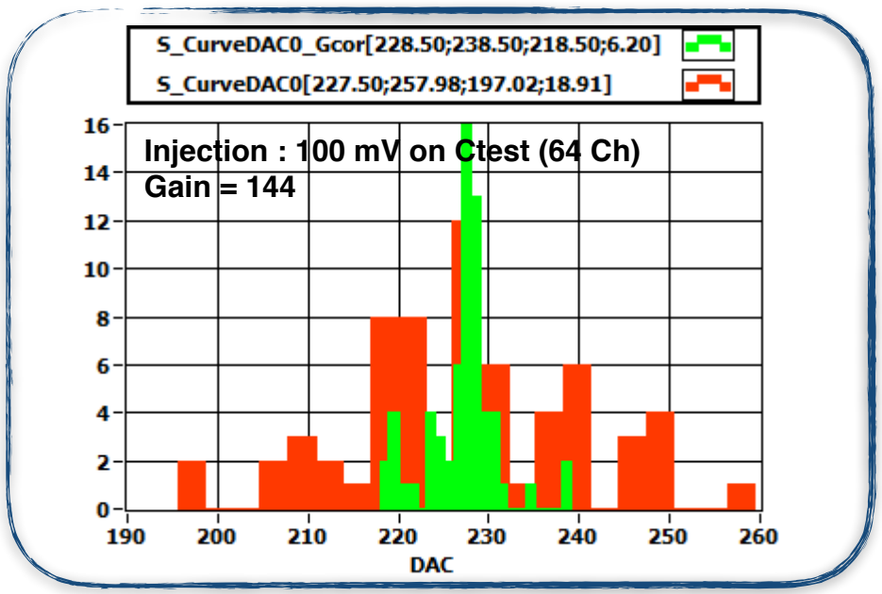
786 tested at IPNLyon - France

Yield : 83.3 %

Majority of discharges : Dead Channels



S-curves for all channels of one HR3, before (red) and after (green) gain correction

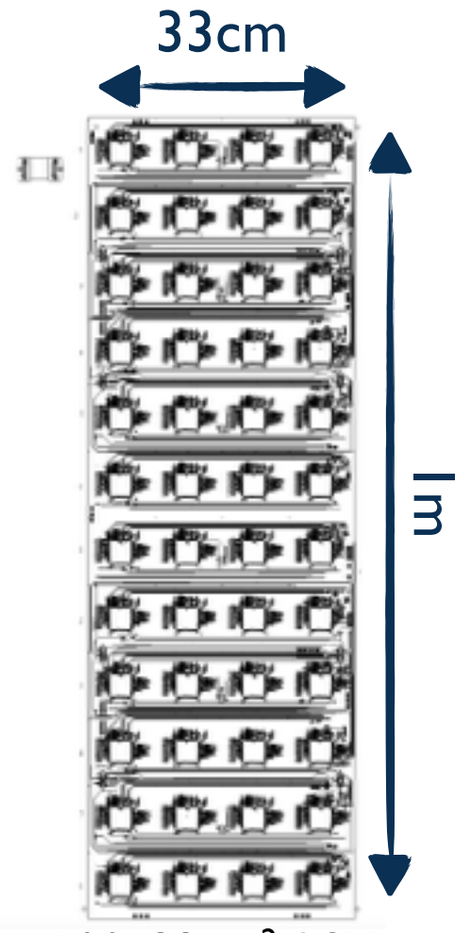


New Electronics - ASU

Size doubled : 100x33cm^2 → Keep 6ASU/chamber

Chinese company (ASICs manufacturer)

Will host 48Asics



100x33cm^2 ASU
with 48 ASICs

New Electronics - ASU

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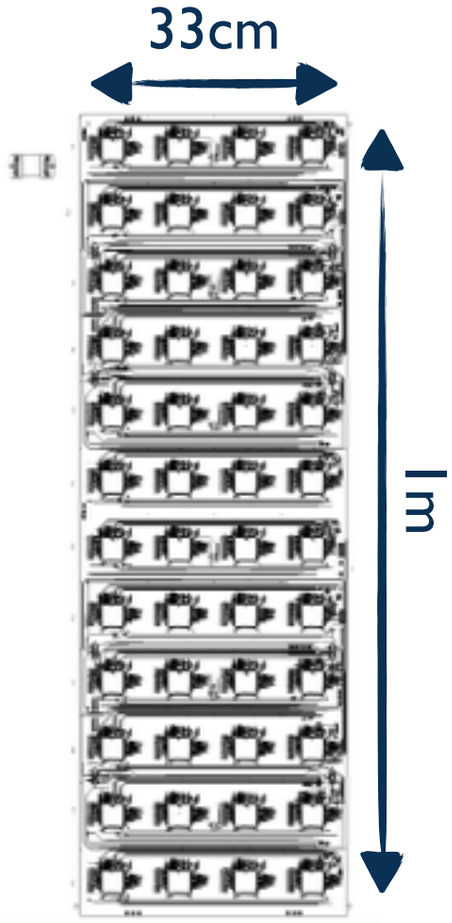
Chinese company (ASICs manufacturer)

Will host 48Asics

Both designs (50x33cm^2 &100x33cm$^{2)}$ are **scalable** to biggest chambers

Final disposition to be decided



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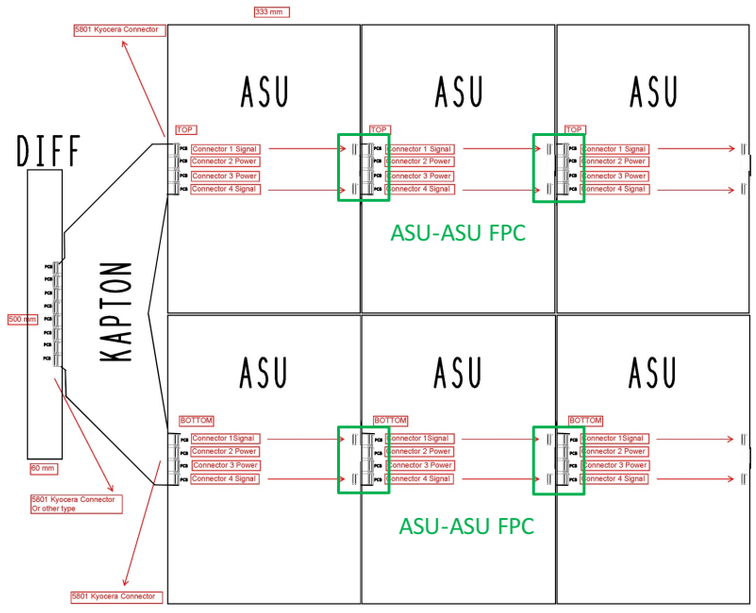

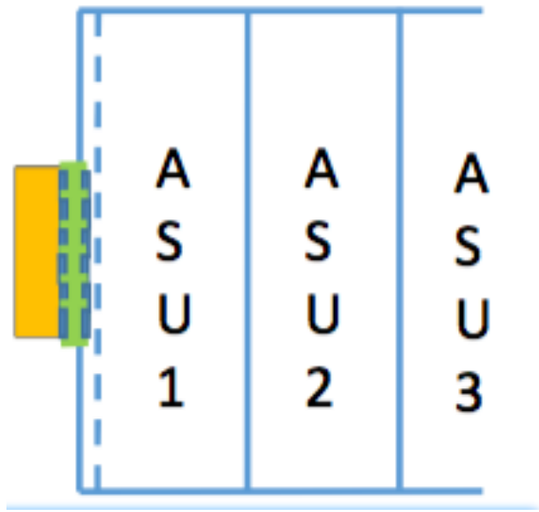

New Electronics - Detector InterFace (DIF)

Send DAQ commands (slow control, clock, etc.) to ASICs

ReadOut data from ASICs to DAQ

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ReadOut data from ASICs to DAQ

Changes:

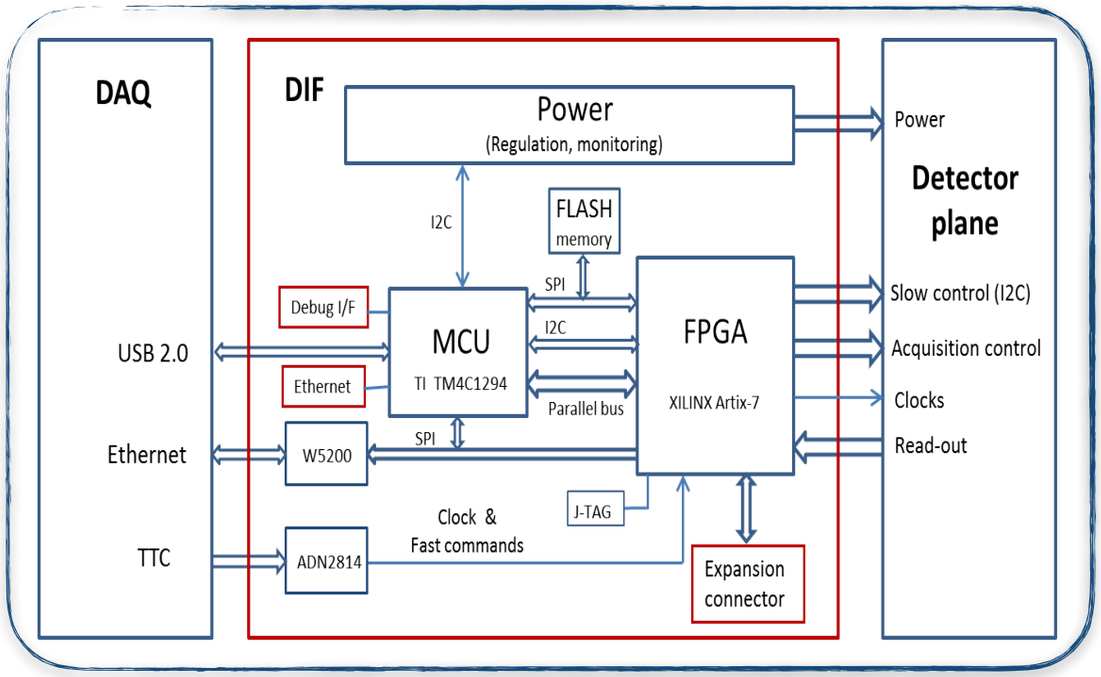
Only one per chamber

↳ DIF handle up to 432 HR3 chips (3x1m2)
(48 HR2 with m3 DIF)

Clock sent via TTC (HDMI before)

Slow control through I2C (vs SR)

Read Out through Ethernet(vs USB)



Block diagram of new SDHCAL DIF

New Electronics - Going DIF Less

Several connection options were/are considered

Direct connection

Cable connection

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Many constraints:

DIF length

Connector position

High number of signals

High current on power pins (30A per plane)

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High current on power pins (30A per plane)

→ **Trouble**

Solution:

Integrate the Dif into a longer PCB

Already achievable

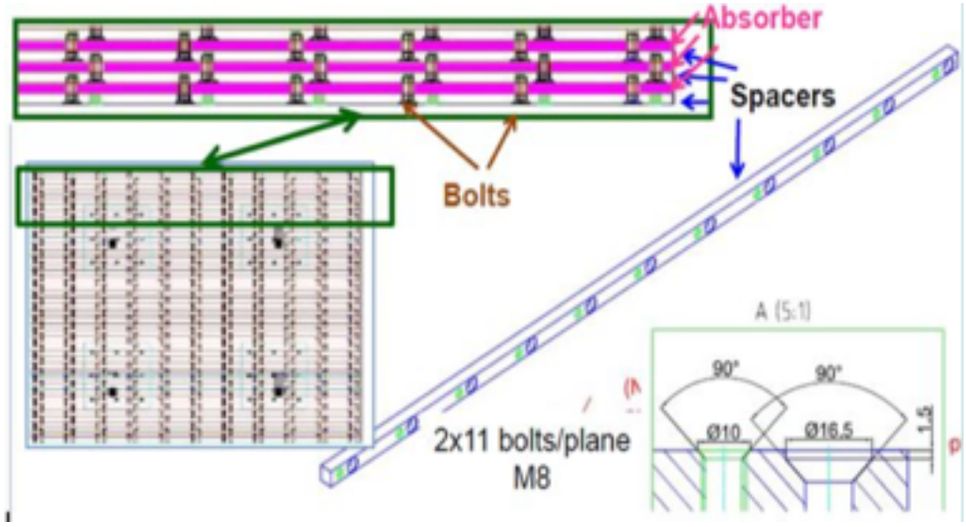
Mechanics

Current prototype

Assembly: Lateral spacers & staggered bolts

Thickness tolerance : 50um

Planarity : 500 um



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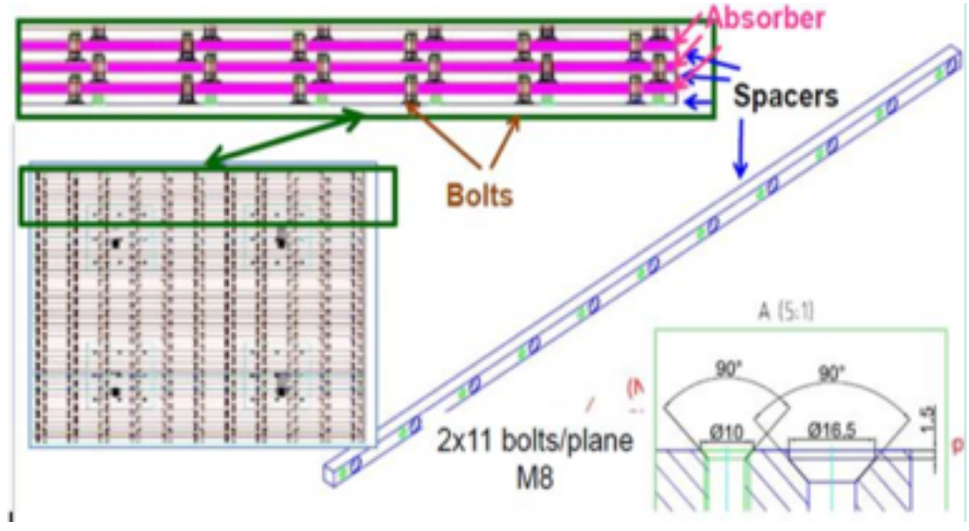
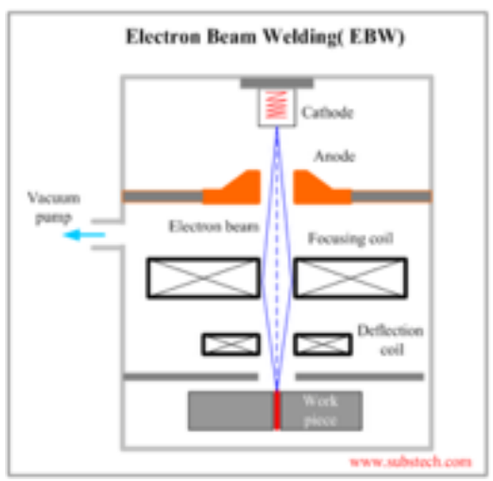


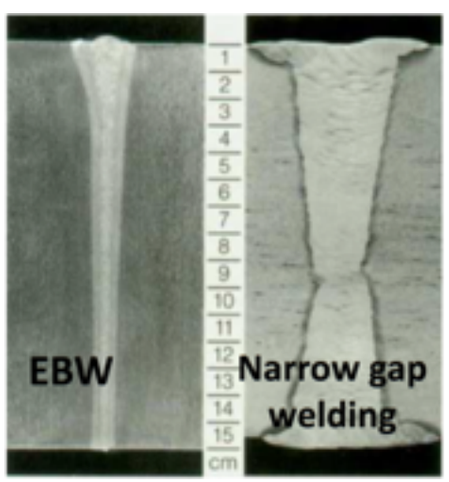
New prototype for 2 & 3m^2 chambers

Electron Beam Welding:

Reduce lateral dimensions

Reduce dead space





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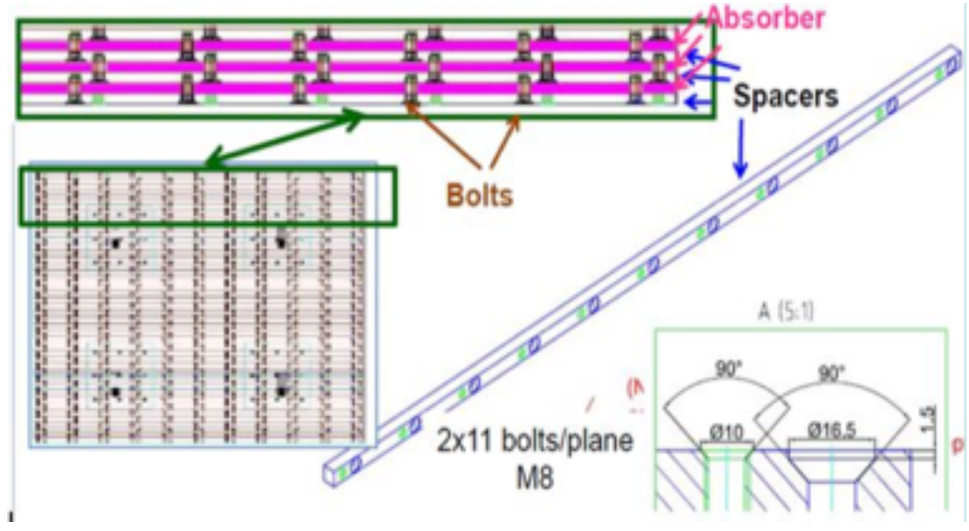

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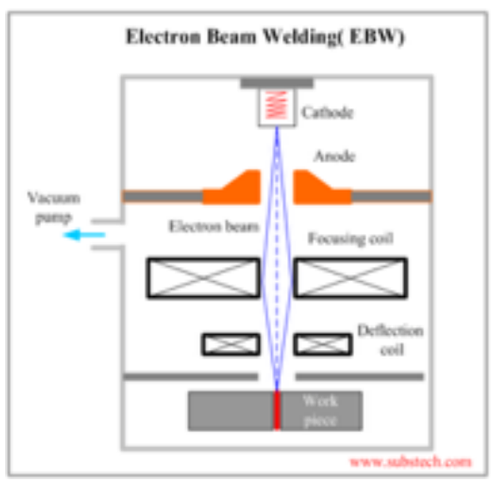
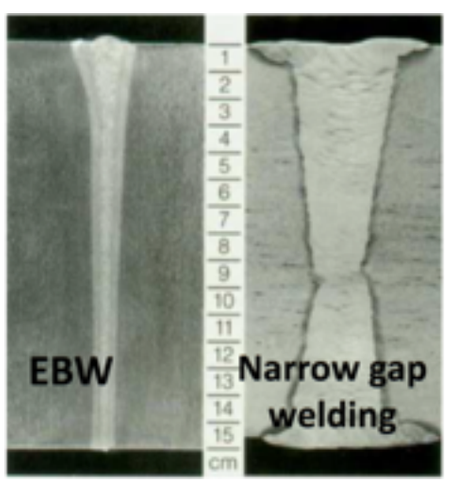
↳ Laser Welding could be used





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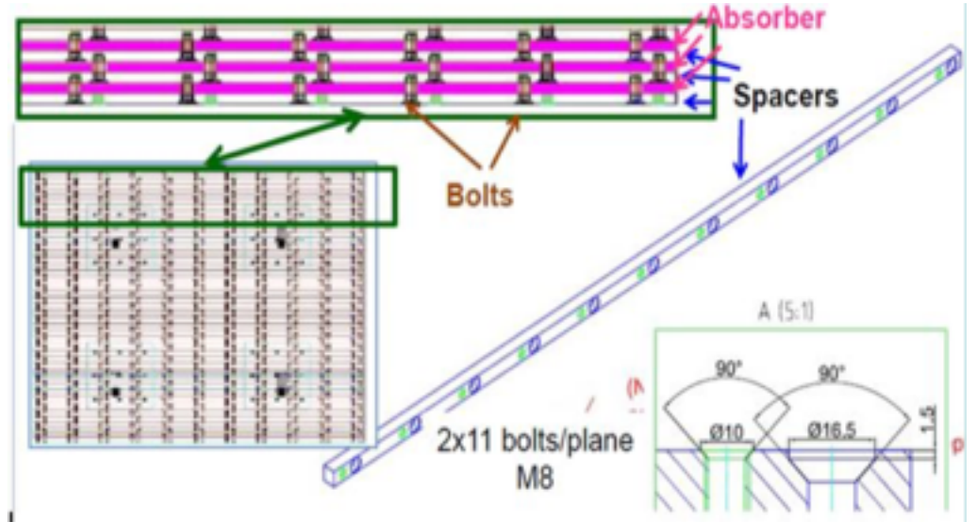

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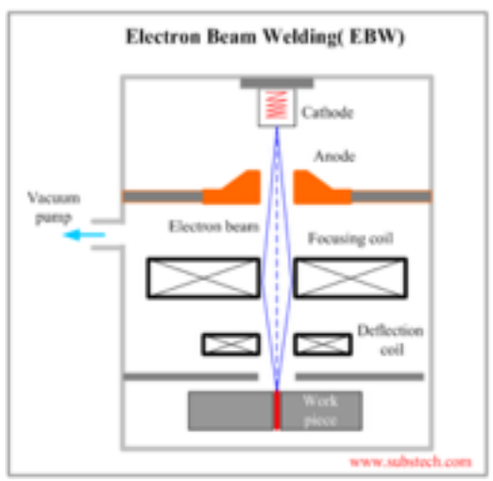

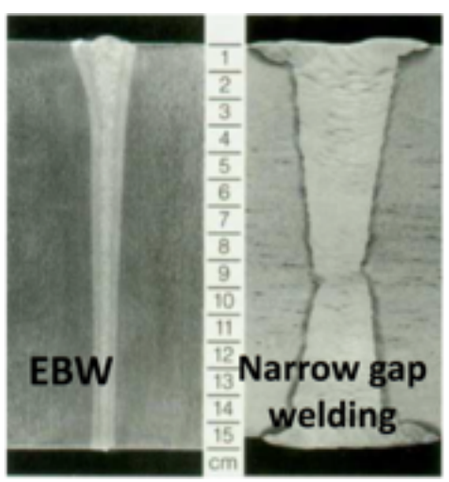

Sub-mm planarity is long & expensive

Roller levelling technique

↳ <0.5mm over 3m achieved

Other Challenges

Cassette

1x1m^2 & 11mm thickness = 70Kg already

Can increase Thickness

Decrease absorber

→ **Stiff but heavy**

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Combined Test Beam

With Ecal in 2016 (Common DAQ, etc.)

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As seen in G. Grenier's talk, SDHCAL prototype behaviour is satisfactory

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New bigger prototype with less planes under advanced development

- New Electronics is being finalised and partly tested
- Mechanics R&D ongoing: Optimisation of production procedures
- Getting closer to the ILD final design
- Construction & testing by 2017

Overview

As seen in G. Grenier's talk, SDHCAL prototype behaviour is satisfactory

New bigger prototype with less planes under advanced development

- New Electronics is being finalised and partly tested
- Mechanics R&D ongoing: Optimisation of production procedures
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Fruitful collaboration between

IPNL, LPC, GWNU, UGent, CIEMAT, UCL & NCEPU

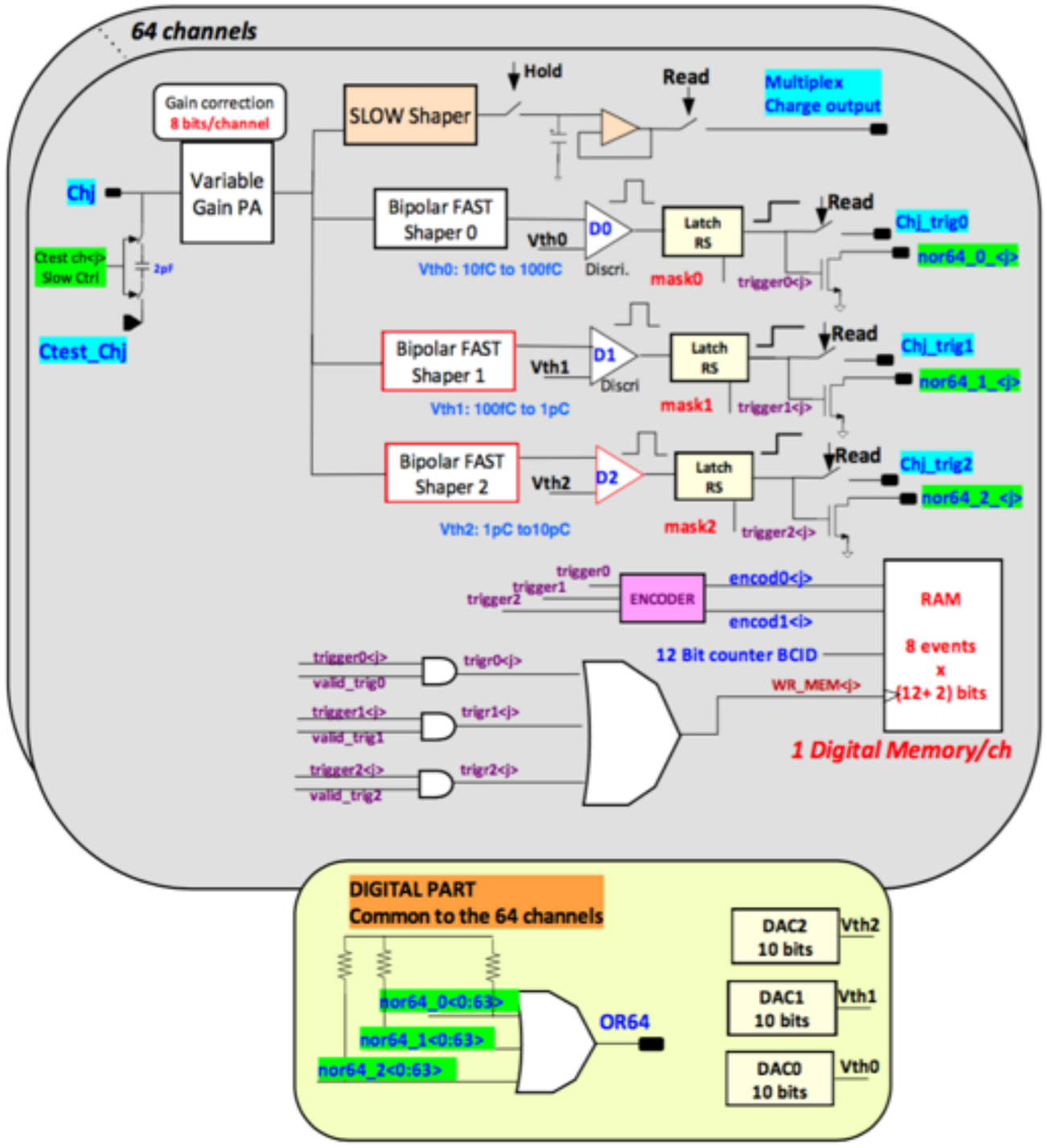
All challenges not yet overcome but results are promising

Backup

Antoine Pingault (@ugent.be)

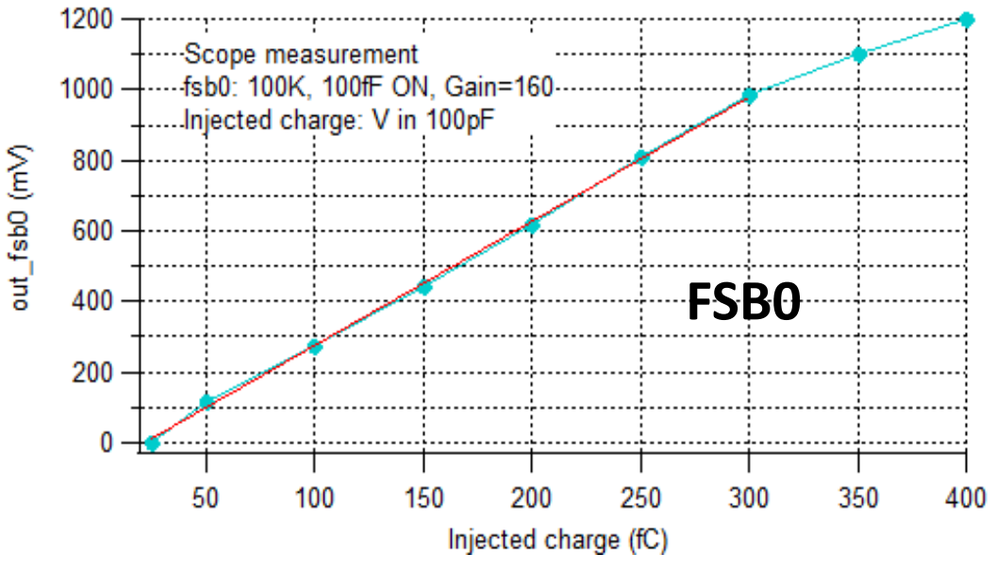
Backup: HR3

- 64 independant channels w/ current amplifiers
- Trigger less mode (auto trigger : 15fC->50pC)
- Gain correction (x2 max)
- 3 shapers + 3 discriminators (2bits included for readout)
- I2C protocol for slow control
- Zero suppression
- Up to 8 events/channel with 12 bit time stamp
- Integrated clock generator: PLL
- Power pulsing mode

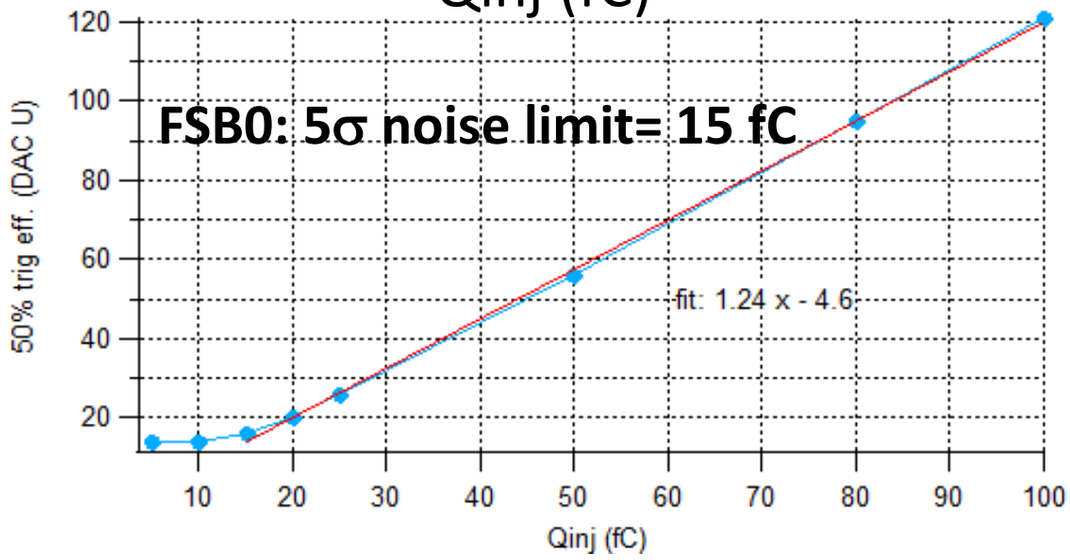


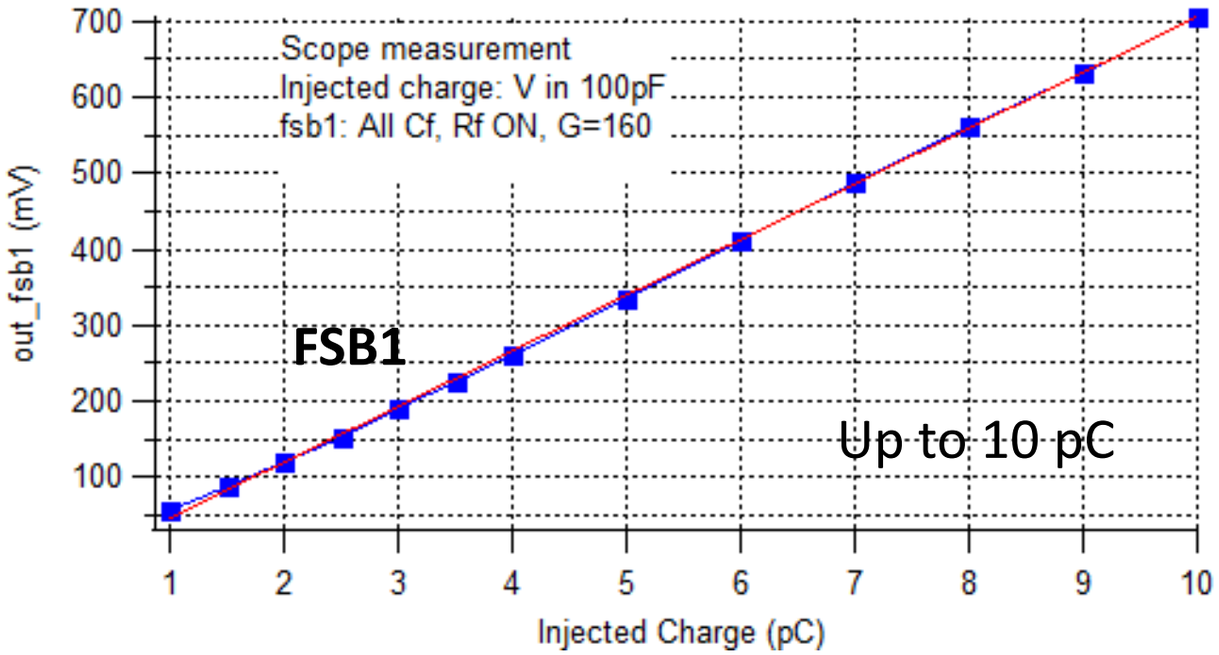
Backup: HR3 - FSB linearity

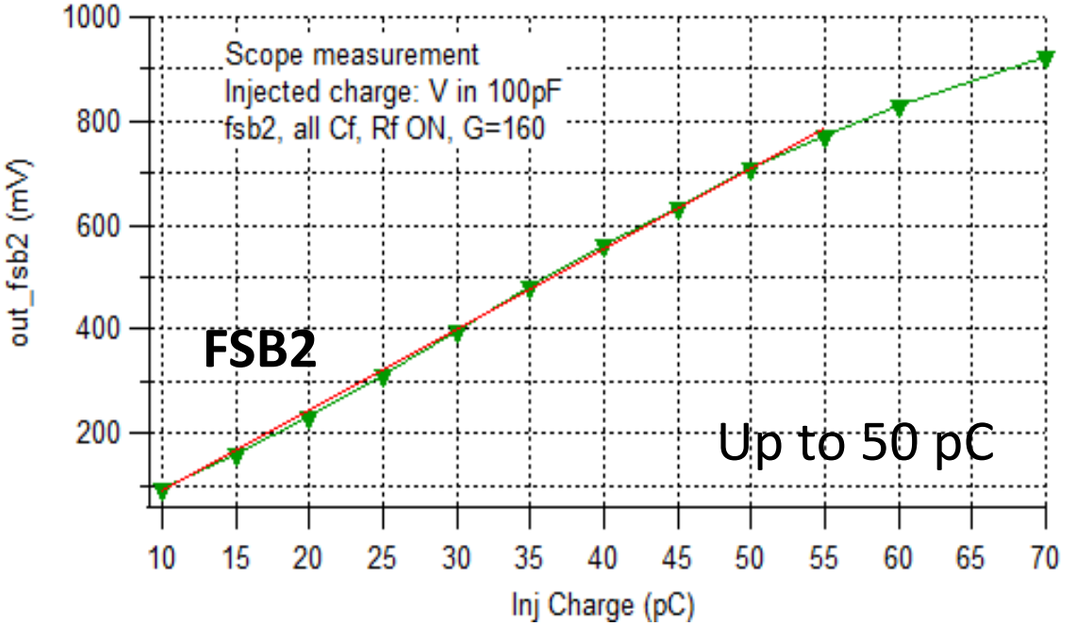
Fast shaper outputs (mV) vs Qinj (fC)



50% trigger efficiency (DAC units) vs Qinj (fC)







Dynamic range: 15fC - 50 pC

Backup: DIF

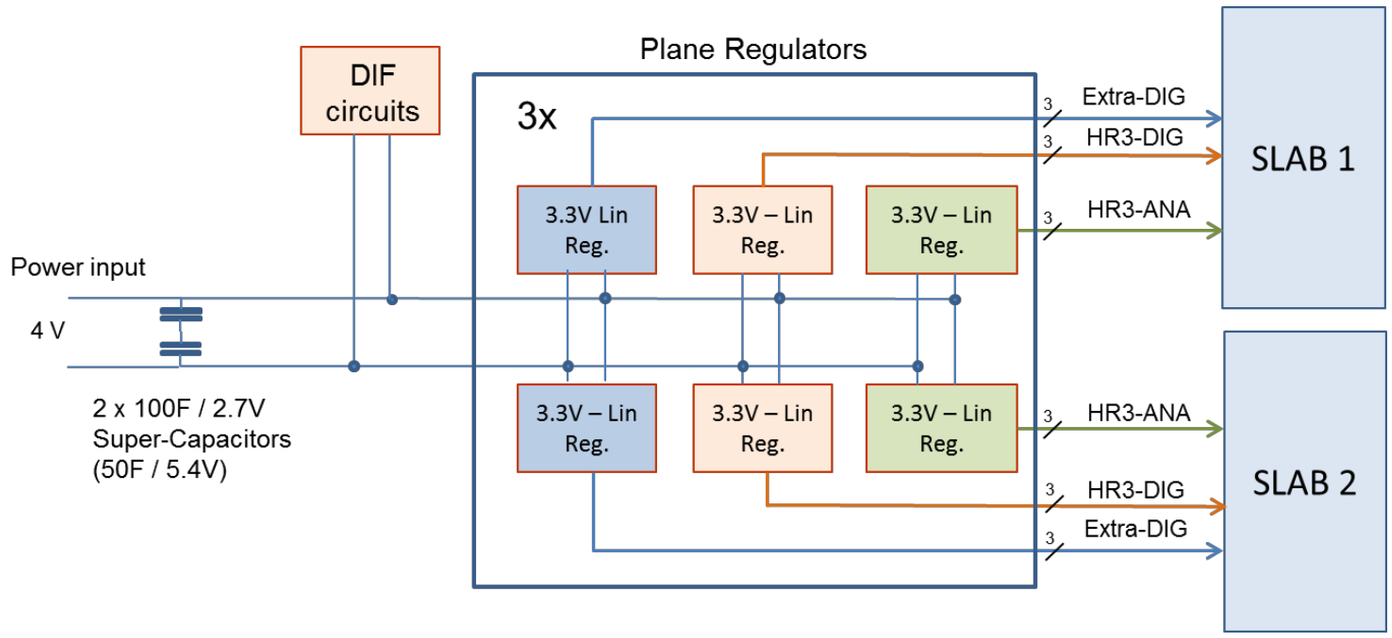
- Only one DIF per plane (instead of three)
  - DIF handle up to 432 HR3 chips (48 HR2 with m3 DIF)
  - HR3 slow control through I2C bus (12 IC2 buses). Keeps also two of the old slow control buses as backup & redundancy.
  - Data transmission to/from DAQ by Ethernet
  - Clock and synchronization by TTC (already used in LHC)
  - 93W Peak power supply with super-capacitors (vs 8,6 W in previous DIF)
  - Spare I/O connectors to the FPGA (i.e. for GBT links)
- • Upgrade USB 1.1 to USB 2.0

Backup: DIF power distribution

DIF to Plane Power distribution

Power mode	Extra circuits	HR3	1m² Plane	3m² Plane
Allways active	8,57	22,39	30,96	92,88
Power-Pulsing (0,5% duty cycle)	4,18	0,112	4,29	12,88

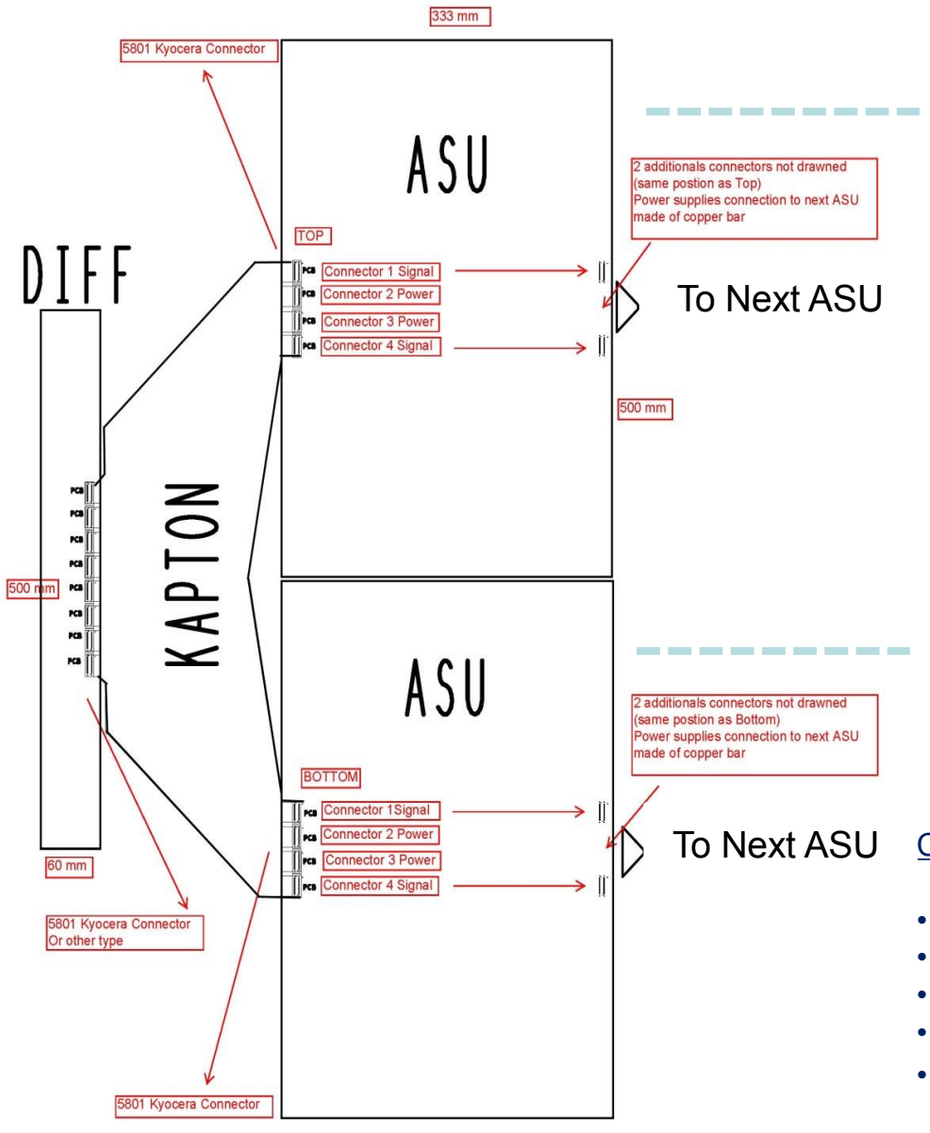
New prototype (3m² & HR3) expected power (W) requirements



- Power distribution to the plane by three power groups per slab (reliability) with three power lines each
- Super-caps at the input for local storage of the peak current needed during the detector sort active period (0.5% of the time). Allow to dimension the global power supply for the average power and not for the peak (85% reduction)
- Low drop-out regulators to minimize the power dissipated.
- Current monitoring and over-current protection per output voltage and slab

Backup: ASU

PROPOSED ASU ARCHITECTURE



Architecture motivations :

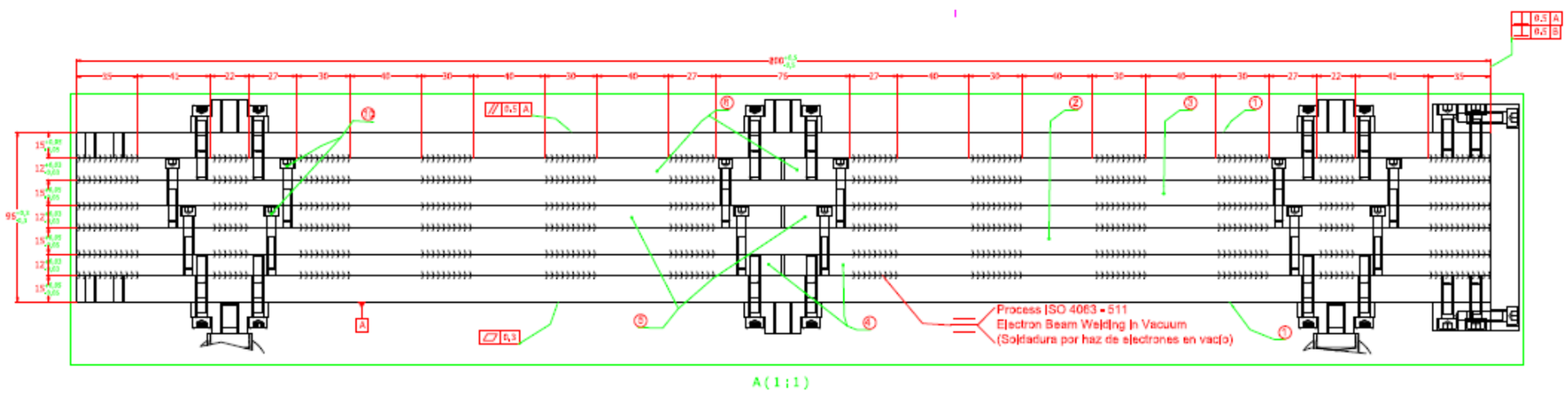
- 6 lines of 4 HR3 per ASU (500 *333 mm^2)
- 12 HR3/Line for 1 m long ASU
- 36 HR3/Line for 3 m long ASU
- Same ASU design for all ASU in a SLAb
- All buffers on DIF side :
  - save power on ASU side
  - easier to cool
- 5801 Kyocera connectors on ASU side (low profile and already used) :
  - 2 for signals
  - 2 for power supplies (up to 24 A)
- DIF to ASU : FPC part with FR4 for Kyocera connectors :
  - Trench on connector side to facilitate connection
  - Connector on DIF side is free (or compatible with Kyocera size)
- ASU to ASU : FPC like in the m^3 prototype
- Man power : only 1 ASU Design, DITF to ASU and ASU to ASU

Connectors : (Kyocera 5801)

- Same assignment for Top and Bottom signal connectors
- New SC and Old one are implemented
- The two I2C port can be used
- Inner PLL or external 40 MHz for state machine
- Tramsmiton/Dout/Start-Readout/EndReadout number 2 can be used : 1 for 2 HR3 line

Backup: EBW

The small prototype was welded by electron beam welding process at CERN.
Tests were then performed on planarity



Backup: Roller levelling

Machining test for the large prototype

The planarity required for the final prototype is <1mm, larger than what was required for the 1m3 prototype but more difficult to obtain in a surface three times bigger

→ One plate of Inox AISI 304 of 2900x950 and 15 mm thickness was produced.

→Operational tool.

→Verification tool.

The plates were produced with a Planarity tolerance below 1 mm in a length of about 2.3 m (but in the rest of the length was 3 mm due to the Machine capability)